



VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

Sponsored by Lavu Educational Society, Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad.
Kondapur (V), Ghatkesar (M), Medchal - Malkajgiri (D) - 501 301 TS INDIA
Phone: +08615 200006/07/08 Email: info@vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VMTW/ECE/AOC/CIR/2018-19/I/03

07-09-2018.

CIRCULAR

This is to inform all the IV B. Tech ECE students that there will be an Add on course on “**Design and FPGA Implementation of DSP Processor using Verilog**” in association with AMTRONICS PVT LTD., Hyderabad, on 11-09-2018 to 29-10-2018 All students are invited to take part in this course. The participating students will be honored with certificates of participation. During the course you will be encouraged to interact with the speaker and the other participants through the case study discussions. Hence those who are interested can sign in registration form.

HOD,ECE.

Copy to

The Principal, for kind information

IQAC

Notice board

IV.B.Tech students

Dept. file

Head of the Department
Electronics and Communication Engineering
Vignan's Institute of Management and Technology for Women
Kondapur (V), Ghatkesar (M), R.R. Dist-501 301



PRINCIPAL

Vignan's Institute of Management & Technology For Women
Kondapur(V),Ghatkesar(M),Medchal-Malkajgiri(Dt)-501301
Telangana State

About the Course:


The digital signal processing (DSP) applications are in numerous infotainments, Medical diagnostics and advanced communication and radar systems. Always the advancements in VLSI technology will have an impact on the performance of these systems. VLSI DSP deals with such architectural and algorithmic optimization techniques to design high-performance DSP systems. As VLSI DSP needs inter-domain expertise of both DSP and VLSI domain, there is a huge necessity to impart the necessary concepts and hands-on skills to research scholars and faculty.

Course Objectives:

- Introduction to DSP VLSI
- Architectural transformation techniques (Retiming, Folding)
- Architectural transformation techniques (Unfolding)
- Numerical Strength reduction techniques
- Hands-on MATLAB for VLSI DSP
- Introduction to INTEL FPGA Design flow
- Introduction to DSP Builder
- Design flow using DSP Builder
- Industry practice and trends in DSP VLSI system Design flow

Expected Outcomes:

- At the end of Workshop, participants will be able to
- Simulate and verify a design.
 - Work with real time projects using Architectural transformation techniques (Retiming, Folding).
 - Work with real time projects using Architectural transformation techniques (Unfolding).
 - Work with real time projects using Numerical Strength reduction techniques.
 - Work with real time projects using DSP Builder.

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ADD-ON COURSE ON
“DESIGN & FPGA
IMPLEMENTATION OF DSP
PROCESSOR USING VERILOG”

11TH SEP TO 29TH OCT, 2018

Duration of the Course: 32 Hrs

Venue:
‘B’-Block Seminar Hall,
VMTW.

Organized By:

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



Resource Person:

Mr. Arjun Mohan

Sr. Engineer,

Amtronics, Hyderabad.

Co-ordinator:

Mr. J. Sunil Kumar,

Assistant Professor, Dept. of ECE,

Contact No: +91 83747 17668

Last Date For Registration: 16th Aug, 2018



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 07-09-2018

B.Tech IV-I SEM

DAY WISE SCHEDULE SHEET

SECTION: ECE-A&B

Room number: BFF6

S.no	DAY	Topic	Timings	Duration
1.	11-09-18	Introduction to embedded	04:00pm to 05:00pm	1 hour
2.	12-09-18	Application Areas	04:00pm to 05:00pm	1 hour
3.	14-09-18	Categories of embedded processors	04:00pm to 05:00pm	1 hour
4.	15-09-18	Hardware architecture	04:00pm to 05:00pm	1 hour
5.	17-09-18	Software architecture	04:00pm to 05:00pm	1 hour
6.	18-09-18	Application software	04:00pm to 05:00pm	1 hour
7.	19-09-18	Communication software	04:00pm to 05:00pm	1 hour
8.	20-09-18	Introduction to Harvard	04:00pm to 05:00pm	1 hour
9.	22-09-18	Architectures	04:00pm to 05:00pm	1 hour
10.	24-09-18	CISC & RISC Architectures	04:00pm to 05:00pm	1 hour
11.	25-09-18	CISC & RISC Architectures	04:00pm to 05:00pm	1 hour
12.	26-09-18	PIC Microcontrollers	04:00pm to 05:00pm	1 hour
13.	27-09-18	Introduction to PIC	04:00pm to 05:00pm	1 hour
14.	28-09-18	Architecture and memory	04:00pm to 05:00pm	1 hour
15.	29-09-18	Registers, I/O ports	04:00pm to 05:00pm	1 hour
16.	01-10-18	Interrupts	04:00pm to 05:00pm	1 hour
17.	03-10-18	Timer, instruction sets	04:00pm to 05:00pm	1 hour
18.	04-10-18	PIC programming in assembly and	04:00pm to 05:00pm	1 hour
19.	05-10-18	Sensor interfacing	04:00pm to 05:00pm	1 hour
20.	06-10-18	Motor control	04:00pm to 05:00pm	1 hour
21.	08-10-18	SPI bus protocols	04:00pm to 05:00pm	1 hour
22.	09-10-18	ARM design philosophy	04:00pm to 05:00pm	1 hour
23.	10-10-18	data flow model and core	04:00pm to 05:00pm	1 hour
24.	11-10-18	ARM processor families	04:00pm to 05:00pm	1 hour
25.	12-10-18	Instruction Sets	04:00pm to 05:00pm	1 hour
26.	13-10-18	Data processing instructions	04:00pm to 05:00pm	1 hour
27.	15-10-18	Addressing modes	04:00pm to 05:00pm	1 hour
28.	16-10-18	conditional instructions	04:00pm to 05:00pm	1 hour
29.	20-10-18	Raspberry Pi	04:00pm to 05:00pm	1 hour
30.	22-10-18	Programming the Raspberry Pi	04:00pm to 05:00pm	1 hour
31.	24-10-18	Communication facilities on	04:00pm to 05:00pm	1 hour



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		Raspberry Pi		
32.	25-10-18	Interfacing of sensors and actuators	04:00pm to 05:00pm	1 hour
33.	27-10-18	Intel Galileo	04:00pm to 05:00pm	1 hour
34.	29-10-18	μ for Embedded System and IoT	04:00pm to 05:00pm	1 hour
35.	29-10-18	Test conducted & Feedback Taken	04:00pm to 05:00pm	1 hour
Total 35 hours				


Coordinator


HOD

Head of the Department
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 11-09-2018

B.Tech IV-I SEM

STUDENT REGISTRATION LIST

SECTION: ECE-A

S.No	Roll number	Name of the student	Signature
1.	15UP1A0401	BEDUDHURI MEGHANA	Meghana
2.	15UP1A0402	C VARSHA REDDY	Varsha
3.	15UP1A0403	CHENNU LAXMI PRASANNA	Laxmi
4.	15UP1A0405	CHILUMULA RACHANA	Rachana
5.	15UP1A0406	CHUNCHU RAMYA SRI	Ramyasri
6.	15UP1A0407	DADI SHIVANJALI	Anjali
7.	15UP1A0408	DEVARAKONDA KEERTHI	Keerthi
8.	15UP1A0409	DEVARAKONDA PREETHI	Preethi
9.	15UP1A0410	DHODLA ALEKHYA	Alekhyasri
10.	15UP1A0411	DUMALA PRIYANKA	Priyanka
11.	15UP1A0412	G VYSHNAVI	Vyshnavi
12.	15UP1A0414	GANGAPURAM HIMAJA	Himaja
13.	15UP1A0415	GOPALADAS MOUNIKA	Mounika
14.	15UP1A0416	GUNDA DEVIKA	Devika
15.	15UP1A0417	GUNTI SRAVANI	Sravani
16.	15UP1A0418	HARIVENKATANAGA HARIPRIYA	Haripriya
17.	15UP1A0419	JAKKIDI PRANAYA	Pranaya
18.	15UP1A0420	KAKANI TEJA SRI	Tejasri
19.	15UP1A0421	KANDADI NIKHITHA	Nikhitha
20.	15UP1A0422	KANDHATI UMA	Uma
21.	15UP1A0423	KETHIREDDY PRATHYUSHA	Prathyusha
22.	15UP1A0424	KODEMALA SAIKRUPA	Saikrupa
23.	15UP1A0425	KOLA SONIA	K.Sonia
24.	15UP1A0426	L VIJITHA	Vijitha
25.	15UP1A0427	MAINELLY NIKHITHA	Nikhitha
26.	15UP1A0428	MALLELA MAMATHA	Mamatha
27.	15UP1A0429	MATTI PALLAVI	Pallavi
28.	15UP1A0430	MOJJA KAVERI	Kaveri
29.	15UP1A0431	MULLAPUDI VENKATA LIKHITA	Likhita
30.	15UP1A0432	PABBA VIKASINI	Vikasini
31.	15UP1A0434	PALADUGULA SRIKAVYA	Kavya
32.	15UP1A0435	PAPINENI BHAVANA	Bhavana
33.	15UP1A0436	PERUGUPALLI VIDYULLEKHA	Vidya



Principal
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34.	15UP1A0437	PINNAPU REDDY RAMYA	Ramya
35.	15UP1A0438	S AMRUTHA VARSHINI	Varshini
36.	15UP1A0439	SALLA VARSHINI	Varshini
37.	15UP1A0440	SAMUDRALA NANDINI	Nandini
38.	15UP1A0401	BEDUDHURI MEGHANA	Meghana
39.	15UP1A0402	C VARSHA REDDY	Varsha
40.	15UP1A0403	CHENNU LAXMI PRASANNA	Prasanna


COORDINATOR


ECE,HOD

Head of the Department
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Date: 11-09-2018

B.Tech IV-I SEM

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SECTION: ECE-A

S.No	Roll number	Name of the student
1.	15UP1A0401	BEDUDHURI MEGHANA
2.	15UP1A0402	C VARSHA REDDY
3.	15UP1A0403	CHENNU LAXMI PRASANNA
4.	15UP1A0405	CHILUMULA RACHANA
5.	15UP1A0406	CHUNCHU RAMYA SRI
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14.	15UP1A0416	GUNDA DEVIKA
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16.	15UP1A0418	HARIVENKATANAGA HARIPRIYA
17.	15UP1A0419	JAKKIDI PRANAYA
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31.	15UP1A0434	PALADUGULA SRIKAVYA
32.	15UP1A0435	PAPINENI BHAVANA
33.	15UP1A0436	PERUGUPALLI VIDYULLEKHA




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38.	15UP1A0401	BEDUDHURI MEGHANA
39.	15UP1A0402	C VARSHA REDDY
40.	15UP1A0403	CHENNU LAXMI PRASANNA


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Academic Year: 2018-19

Date: 11-09-2018

B.Tech IV-I

STUDENT REGISTRATION LIST

SECTION: ECE-B

S.No	Roll number	Name of the student	Signature
1.	15UP1A0441	SUDAGANI SWETHA	Swetha
2.	15UP1A0442	VONTARI ARCHANA	Archana
3.	15UP1A0443	MANASA REDDY BODELA	Manasa
4.	15UP1A0444	BALA THARUNA KEERTHI	Keerthi
5.	15UP1A0445	BANALA PRIYANKA	Priyanka
6.	15UP1A0446	BANGARAM MAMATHA	Mamatha
7.	15UP1A0447	BASIREDDY BHARATHI REDDY	Bharathi
8.	15UP1A0448	BILLAKANTI RAVALI	Ravali
9.	15UP1A0449	DEEKONDA SUGANDHA	Su
10.	15UP1A0450	GADDAM JOSHNA	Joshna
11.	15UP1A0451	GOGINENI NIKITHA	G. Nikitha
12.	15UP1A0452	GUNDAGANI NAGASHIRISHA	Sirisha
13.	15UP1A0453	JALA MOUNIKA	JA
14.	15UP1A0454	K RAMYA REDDY	K. Ravi
15.	15UP1A0455	KANALA KAVYA REDDY	Kavya
16.	15UP1A0456	KANDUKURI SRAVYA	Sravya
17.	15UP1A0457	KARNATI SRIHARSHA	Harsha
18.	15UP1A0458	KASULA NAVYA SRI	Navya
19.	15UP1A0459	KETHIREDDY RAMYA	Ravi
20.	15UP1A0460	KOMATIREDDY SIRIJA	Sirija
21.	15UP1A0461	LAVANYA SEELAM	Lavanya
22.	15UP1A0462	M HARICHANDANA	Chandana
23.	15UP1A0463	MAHAJAN SRADHA	Sr
24.	15UP1A0464	MANCHALA SHIVAPRIYA	Shiva Priya
25.	15UP1A0465	MANTIPALLY PRAVALIKA	Pravalika
26.	15UP1A0466	METTU SRAVANTHI	Sravanthi
27.	15UP1A0467	MUNAGALA YASHASWINI	M. Yash
28.	15UP1A0468	NAGANOLLU ANUSHA REDDY	Anusha
29.	15UP1A0469	PACHA VEDASRI	Veda
30.	15UP1A0470	VENKATA YASHASWINI	Yash
31.	15UP1A0472	POCHAMPALLY PRIYANKA	Priya
32.	15UP1A0473	POTHEPAKA MANASA	Manasa
33.	15UP1A0474	SHEELA NIKITHA	Nikitha




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34.	15UP1A0475	SHERIKAR PRIYANKA	<i>S. Priyanka</i>
35.	15UP1A0476	SHIVA NIKHITHA	<i>Nikhitha</i>
36.	15UP1A0477	SUNKI KALYANI	<i>Kalyani</i>
37.	15UP1A0478	VEMURI MAHATHI	<i>Mahathi</i>
38.	15UP1A0479	YASA MINISHA REDDY	<i>Minisha</i>
39.	15UP1A0480	YERUVA SAGAR BALA DIVYA	<i>Y. Divya</i>


COORDINATOR


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Academic Year: 2018-19

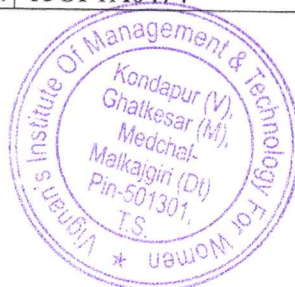
Date: 11-09-2018

B.Tech IV-I SEM

STUDENT REGISTERED LIST

SECTION: ECE-B

S.No	Roll number	Name of the student
1.	15UP1A0441	SUDAGANI SWETHA
2.	15UP1A0442	VONTARI ARCHANA
3.	15UP1A0443	MANASA REDDY BODELA
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32.	15UP1A0472	POCHAMPALLY PRIYANKA
33.	15UP1A0473	POTHEPAKA MANASA
34.	15UP1A0474	SHEELA NIKITHA



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B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	11-09-18	12-09-18	14-09-18	15-09-18	17-09-18
1.	15UP1A0401	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
2.	15UP1A0402	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ranya	Ranya	Ranya	Ranya	Ranya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10.	15UP1A0411	Poivyanka	Poivyanka	Poivyanka	Poivyanka	Poivyanka
11.	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Tejasri	Tejasri	Tejasri	Tejasri	Tejasri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	K.Sonia	K.Sonia	K.Sonia	K.Sonia	K.Sonia
24.	15UP1A0426	Vijitha	Vijitha	Vijitha	Vijitha	Vijitha
25.	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Hikunti	Hikunti	Hikunti	Hikunti	Hikunti
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
33.	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya



[Signature]
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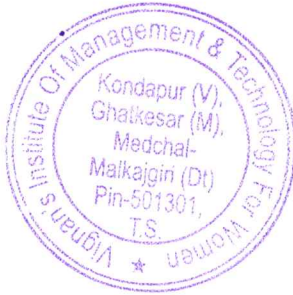
Vignans Institute of Management & Technology For Women
Kondapur(V), Ghatkesar(M), Medchal-Malkajgiri(D)-501301
Telangana State

34.	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
35.	15UP1A0438	Varshini	Varshini	Varshini	Varshini	Varshini
36.	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
40.	15UP1A0403	prassanna	prassanna	prassanna	prassanna	prassanna


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Head of the Department
Electronics and Communication Engineering
Vignan's Institute of Management and Technology for Women
Kondapur (V), Ghatkesar (M), R.R. Dist-501 301




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Phone: +08615 200006/07/08 Email: info@vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 11-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	11-09-18	12-09-18	14-09-18	15-09-18	17-09-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
7.	15UP1A0447	Bhargathi	Bhargathi	Bhargathi	Bhargathi	Bhargathi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	Sw	Sw	Sw	Sw	Sw
10.	15UP1A0450	Joshua	Joshua	Joshua	Joshua	Joshua
11.	15UP1A0451	G.Nikitha	G.Nikitha	G.Nikitha	G.Nikitha	G.Nikitha
12.	15UP1A0452	Srishta	Srishta	Srishta	Srishta	Srishta
13.	15UP1A0453					
14.	15UP1A0454	K.Raj	K.Raj	K.Raj	K.Raj	K.Raj
15.	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
16.	15UP1A0456	Aranya	Aranya	Aranya	Aranya	Aranya
17.	15UP1A0457	Harsha	Harsha	Harsha	Harsha	Harsha
18.	15UP1A0458	Navya	Navya	Navya	Navya	Navya
19.	15UP1A0459	Pooja	Pooja	Pooja	Pooja	Pooja
20.	15UP1A0460	Sirija	Sirija	Sirija	Sirija	Sirija
21.	15UP1A0461	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
22.	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
23.	15UP1A0463	Sh	Sh	Sh	Sh	Sh
24.	15UP1A0464	Shivapriya	Shivapriya	Shivapriya	Shivapriya	Shivapriya
25.	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
26.	15UP1A0466	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
27.	15UP1A0467	M.Yasr	M.Yasr	M.Yasr	M.Yasr	M.Yasr
28.	15UP1A0468	Anusha	Anusha	Anusha	Anusha	Anusha
29.	15UP1A0469	Veda	Veda	Veda	Veda	Veda
30.	15UP1A0470	Yash	Yash	Yash	Yash	Yash
31.	15UP1A0472	Paiya	Paiya	Paiya	Paiya	Paiya
32.	15UP1A0473	Manasa	Manasa	Manasa	Manasa	Manasa
33.	15UP1A0474	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha




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34.	15UP1A0475	A-priyanka	A-priyanka	A-priyanka	A-priyanka	A-priyanka
35.	15UP1A0476	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
36.	15UP1A0477	Kalyani	Kalyani	Kalyani	Kalyani	Kalyani
37.	15UP1A0478	Mahathu	Mahathu	Mahathu	Mahathu	Mahathu
38.	15UP1A0479	Minisha	Minisha	Minisha	Minisha	Minisha
39.	15UP1A0480	Y.Pf	Y.Pf	Y.Pf	Y.Pf	Y.Pf


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 18-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	18-09-18	19-09-18	20-09-18	20-09-18	22-09-18
1.	15UP1A0401	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
2.	15UP1A0402	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekhy	Alekhy	Alekhy	Alekhy	Alekhy
10.	15UP1A0411	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
11.	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Harpriya	Harpriya	Harpriya	Harpriya	Harpriya
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Teja Sri	Teja Sri	Teja Sri	Teja Sri	Teja Sri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	K.Sonia	K.Sonia	K.Sonia	K.Sonia	K.Sonia
24.	15UP1A0426	Vijf	Vijf	Vijf	Vijf	Vijf
25.	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Lipika	Lipika	Lipika	Lipika	Lipika
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
33.	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya



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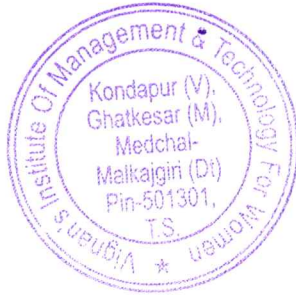
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Telangana State

34.	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
35.	15UP1A0438	Varshini	Varshini	Varshini	Varshini	Varshini
36.	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
40.	15UP1A0403	prassanna	prassanna	prassanna	prassanna	prassanna


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

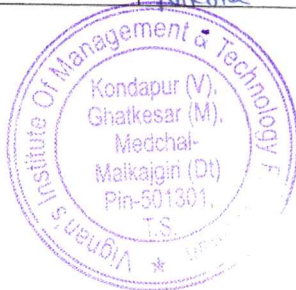
Date: 18-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	18-09-18	19-09-18	20-09-18	20-09-18	22-09-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keelthi	Keelthi	Keelthi	Keelthi	Keelthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
7.	15UP1A0447	Bhavathi	Bhavathi	Bhavathi	Bhavathi	Bhavathi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	Su	Su	Su	Su	Su
10.	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
11.	15UP1A0451	Si.Nikitha	Si.Nikitha	Si.Nikitha	Si.Nikitha	Si.Nikitha
12.	15UP1A0452	Siisha	Siisha	Siisha	Siisha	Siisha
13.	15UP1A0453	AD	AD	AD	AD	AD
14.	15UP1A0454	K.Puf	K.Puf	K.Puf	K.Puf	K.Puf
15.	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
16.	15UP1A0456	Sravya	Sravya	Sravya	Sravya	Sravya
17.	15UP1A0457	Harsha	Harsha	Harsha	Harsha	Harsha
18.	15UP1A0458	Nanya	Nanya	Nanya	Nanya	Nanya
19.	15UP1A0459	Puf	Puf	Puf	Puf	Puf
20.	15UP1A0460	Sirija	Sirija	Sirija	Sirija	Sirija
21.	15UP1A0461	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
22.	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
23.	15UP1A0463	St	St	St	St	St
24.	15UP1A0464	shivaPriya	shivaPriya	shivaPriya	shivaPriya	shivaPriya
25.	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
26.	15UP1A0466	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
27.	15UP1A0467	M.Yas	M.Yas	M.Yas	M.Yas	M.Yas
28.	15UP1A0468	Anusha	Anusha	Anusha	Anusha	Anusha
29.	15UP1A0469	Veda	Veda	Veda	Veda	Veda
30.	15UP1A0470	Yash	Yash	Yash	Yash	Yash
31.	15UP1A0472	priya	priya	priya	priya	priya
32.	15UP1A0473	Manasa	Manasa	Manasa	Manasa	Manasa
33.	15UP1A0474	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha



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34.	15UP1A0475	d.priyanka	d.priyanka	d.priyanka	d.priyanka	d.priyanka
35.	15UP1A0476	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
36.	15UP1A0477	kalyani	kalyani	kalyani	kalyani	kalyani
37.	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
38.	15UP1A0479	Nirisha	Nirisha	Nirisha	Nirisha	Nirisha
39.	15UP1A0480	Y.Def	Y.Def	Y.Def	Y.Def	Y.Def


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

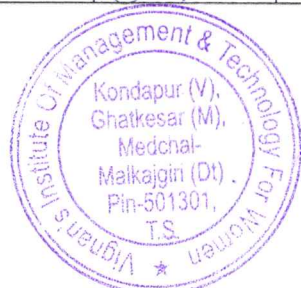
Date: 24-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	24-09-18	25-09-18	26-09-18	27-09-18	28-09-18
1.	15UP1A0401	Ramya	Ramya	Ramya	Ramya	Ramya
2.	15UP1A0402	Vaaha	Vaaha	Vaaha	Vaaha	Vaaha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	Keethi	Keethi	Keethi	Keethi	Keethi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekha	Alekha	Alekha	Alekha	Alekha
10.	15UP1A0411	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
11.	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Hanpriya	Hanpriya	Hanpriya	Hanpriya	Hanpriya
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Tejasri	Tejasri	Tejasri	Tejasri	Tejasri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	k.Sonia	k.Sonia	k.Sonia	k.Sonia	k.Sonia
24.	15UP1A0426	Vijetha	Vijetha	Vijetha	Vijetha	Vijetha
25.	15UP1A0427	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Hikethi	Hikethi	Hikethi	Hikethi	Hikethi
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
33.	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
34.	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya



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35.	15UP1A0438	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
36.	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Vaishya	Vaishya	Vaishya	Vaishya	Vaishya
40.	15UP1A0403	Prasanna	Prasanna	Prasanna	Prasanna	Prasanna


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 24-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	24-09-18	25-09-18	26-09-18	27-09-18	28-09-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
7.	15UP1A0447	Bhavanthi	Bhavanthi	Bhavanthi	Bhavanthi	Bhavanthi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	Sw	Sw	Sw	Sw	Sw
10.	15UP1A0450	Joshua	Joshua	Joshua	Joshua	Joshua
11.	15UP1A0451	Trinikitha	Trinikitha	Trinikitha	Trinikitha	Trinikitha
12.	15UP1A0452	Srishta	Srishta	Srishta	Srishta	Srishta
13.	15UP1A0453	Ne	Ne	Ne	Ne	Ne
14.	15UP1A0454	K.Puf	K.Puf	K.Puf	K.Puf	K.Puf
15.	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
16.	15UP1A0456	Saavya	Saavya	Saavya	Saavya	Saavya
17.	15UP1A0457	Harsha	Harsha	Harsha	Harsha	Harsha
18.	15UP1A0458	Navya	Navya	Navya	Navya	Navya
19.	15UP1A0459	Puif	Puif	Puif	Puif	Puif
20.	15UP1A0460	Sirija	Sirija	Sirija	Sirija	Sirija
21.	15UP1A0461	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
22.	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
23.	15UP1A0463	St	St	St	St	St
24.	15UP1A0464	Shivapriya	Shivapriya	Shivapriya	Shivapriya	Shivapriya
25.	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
26.	15UP1A0466	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
27.	15UP1A0467	M.Yas	M.Yas	M.Yas	M.Yas	M.Yas
28.	15UP1A0468	Anusha	Anusha	Anusha	Anusha	Anusha
29.	15UP1A0469	Veda	Veda	Veda	Veda	Veda
30.	15UP1A0470	Yash	Yash	Yash	Yash	Yash
31.	15UP1A0472	paia	paia	paia	paia	paia
32.	15UP1A0473	Manasa	Manasa	Manasa	Manasa	Manasa
33.	15UP1A0474	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
34.	15UP1A0475	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka



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Telangana State

35.	15UP1A0476	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha.
36.	15UP1A0477	Kalyani	Kalyani	Kalyani	Kalyani	Kalyani
37.	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi.
38.	15UP1A0479	Minisha	Minisha	Minisha	Minisha	Minisha.
39.	15UP1A0480	Y. Puf	Y. Puf	Y. Puf	Y. Puf	Y. Puf


COORDINATOR


ECE, HOD

Head of the Department
Electronics and Communication Engineering
 Vignan's Institute of Management and Technology for Women
 Kondapur (V), Ghatkesar (M), R.R. Dist-501 301




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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 29-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	29-09-18	01-10-18	03-10-18	04-10-18	05-10-18
1.	15UP1A0401	Kavya	Kavya	Kavya	Kavya	Kavya
2.	15UP1A0402	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10.	15UP1A0411	Paiyanka	Paiyanka	Paiyanka	Paiyanka	Paiyanka
11.	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Hanipriya	Hanipriya	Hanipriya	Hanipriya	Hanipriya
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Tejasri	Tejasri	Tejasri	Tejasri	Tejasri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	K. Sonia	K. Sonia	K. Sonia	K. Sonia	K. Sonia
24.	15UP1A0426	Vijj	Vijj	Vijj	Vijj	Vijj
25.	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Lilyt	Lilyt	Lilyt	Lilyt	Lilyt
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
33.	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
34.	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya



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35.	15UP1A0438	Vaishini	Varshini	Varshini	Varshini	Varshini
36.	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
40.	15UP1A0403	prassana	prassana	prassana	prassana	prassana


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

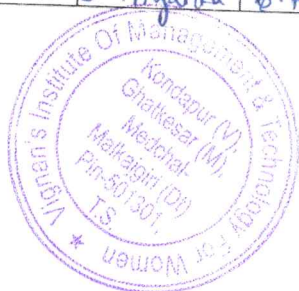
Date: 29-09-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	29-09-18	01-10-18	03-10-18	04-10-18	05-10-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
7.	15UP1A0447	Bhawalathi	Bhawalathi	Bhawalathi	Bhawalathi	Bhawalathi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	Sw	Sw	Sw	Sw	Sw
10.	15UP1A0450	Joshua	Joshua	Joshua	Joshua	Joshua
11.	15UP1A0451	G. Nikitha	G. Nikitha	G. Nikitha	G. Nikitha	G. Nikitha
12.	15UP1A0452	Srishta	Srishta	Srishta	Srishta	Srishta
13.	15UP1A0453	K. Ravi	K. Ravi	K. Ravi	K. Ravi	K. Ravi
14.	15UP1A0454	Kavya	Kavya	Kavya	Kavya	Kavya
15.	15UP1A0455	Sravya	Sravya	Sravya	Sravya	Sravya
16.	15UP1A0456	Harsha	Harsha	Harsha	Harsha	Harsha
17.	15UP1A0457	Navya	Navya	Navya	Navya	Navya
18.	15UP1A0458	Pooja	Pooja	Pooja	Pooja	Pooja
19.	15UP1A0459	Srija	Srija	Srija	Srija	Srija
20.	15UP1A0460	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
21.	15UP1A0461	Chandana	Chandana	Chandana	Chandana	Chandana
22.	15UP1A0462	Shivapriya	Shivapriya	Shivapriya	Shivapriya	Shivapriya
23.	15UP1A0463	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
24.	15UP1A0464	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
25.	15UP1A0465	M. Yas	M. Yas	M. Yas	M. Yas	M. Yas
26.	15UP1A0466	Anusha	Anusha	Anusha	Anusha	Anusha
27.	15UP1A0467	Veda	Veda	Veda	Veda	Veda
28.	15UP1A0468	Yash	Yash	Yash	Yash	Yash
29.	15UP1A0469	Praya	Praya	Praya	Praya	Praya
30.	15UP1A0470	Manasa	Manasa	Manasa	Manasa	Manasa
31.	15UP1A0471	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
32.	15UP1A0472	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
33.	15UP1A0473					
34.	15UP1A0475					



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35.	15UP1A0476	Nikitha	NiEitha	NiEitha	Nikitha	NiEitha
36.	15UP1A0477	kalyani	kalyani	kalyani	kalyani	kalyani
37.	15UP1A0478	Mahalle	Mahalle	Mahalle	Mahalle	Mahalle
38.	15UP1A0479	Minisha	Minisha	Minisha	Minisha	Minisha
39.	15UP1A0480	Y. ees	Y. eef	Y. eef	Y. eef	Y. eef


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Head of the Department
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 06-10-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	06-10-18	08-10-18	09-10-18	10-10-18	11-10-18
1.	15UP1A0401	Ma	Ma	Ma	Ma	Ma
2.	15UP1A0402	vaaha	vaaha	vaaha	vaaha	vaaha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ranya	Ranya	Ranya	Ranya	Ranya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	keerthi	keerthi	keerthi	keerthi	keerthi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekhy	Alekhy	Alekhy	Alekhy	Alekhy
10.	15UP1A0411	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
11.	15UP1A0412	vishnavi	vishnavi	vishnavi	vishnavi	vishnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Harpriya	Harpriya	Harpriya	Harpriya	Harpriya
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Teja Sri	Teja Sri	Teja Sri	Teja Sri	Teja Sri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	k.Sonia	k.Sonia	k.Sonia	k.Sonia	k.Sonia
24.	15UP1A0426	Vidya	Vidya	Vidya	Vidya	Vidya
25.	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Linyt	Linyt	Linyt	Linyt	Linyt
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
33.	15UP1A0436	Vidya	vidyu	vidyu	vidyu	Vidyu



Principal
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34.	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
35.	15UP1A0438	Varshini	Varshini	Varshini	Varshini	Varshini
36.	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
40.	15UP1A0403	Prassanna	Prassanna	Prassanna	Prassanna	Prassanna


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

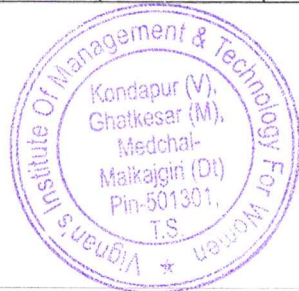
Date: 06-10-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	06-10-18	08-10-18	09-10-18	10-10-18	11-10-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keelthi	Keelthi	Keelthi	Keelthi	Keelthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Manamatha	Manamatha	Manamatha	Manamatha	Manamatha
7.	15UP1A0447	Bhavarthi	Bhavarthi	Bhavarthi	Bhavarthi	Bhavarthi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	Su	Su	Su	Su	Su
10.	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
11.	15UP1A0451	G.N. Nikitha	G.N. Nikitha	G.N. Nikitha	G.N. Nikitha	G.N. Nikitha
12.	15UP1A0452	Shrisha	Shrisha	Shrisha	Shrisha	Shrisha
13.	15UP1A0453	Pa	Pa	Pa	Pa	Pa
14.	15UP1A0454	K. Puf	K. Puf	K. Puf	K. Puf	K. Puf
15.	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
16.	15UP1A0456	Saavya	Saavya	Saavya	Saavya	Saavya
17.	15UP1A0457	Harsha	Harsha	Harsha	Harsha	Harsha
18.	15UP1A0458	Navya	Navya	Navya	Navya	Navya
19.	15UP1A0459	Puf	Puf	Puf	Puf	Puf
20.	15UP1A0460	Sirija	Sirija	Sirija	Sirija	Sirija
21.	15UP1A0461	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
22.	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
23.	15UP1A0463	Sh	Sh	Sh	Sh	Sh
24.	15UP1A0464	Shivapriya	Shivapriya	Shivapriya	Shivapriya	Shivapriya
25.	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
26.	15UP1A0466	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
27.	15UP1A0467	M. Yas	M. Yas	M. Yas	M. Yas	M. Yas
28.	15UP1A0468	Anusha	Anusha	Anusha	Anusha	Anusha
29.	15UP1A0469	Veda	Veda	Veda	Veda	Veda
30.	15UP1A0470	Yash	Yash	Yash	Yash	Yash
31.	15UP1A0472	Priya	Priya	Priya	Priya	Priya
32.	15UP1A0473	Manasa	Manasa	Manasa	Manasa	Manasa
33.	15UP1A0474	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha



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Telangana State

34.	15UP1A0475	S. priyanka	d. priyanka	S. priyanka	S. priyanka	S. priyanka
35.	15UP1A0476	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
36.	15UP1A0477	kalyani	kalyani	kalyani	kalyani	kalyani
37.	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
38.	15UP1A0479	Minisha	Minisha	Minisha	Minisha	Minisha
39.	15UP1A0480	Y. Puf	Y. Puf	Y. Puf	Y. Puf	Y. Puf


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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

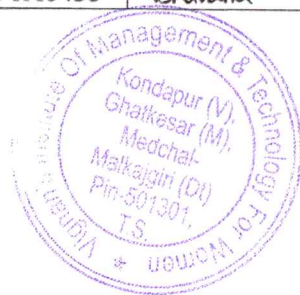
Date: 15-10-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	15-10-18	16-10-18	20-10-18	22-10-18	23-10-18
1.	15UP1A0401	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
2.	15UP1A0402	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10.	15UP1A0411	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
11.	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Hanipriya	Hanipriya	Hanipriya	Hanipriya	Hanipriya
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Teja Sri	Teja Sri	Teja Sri	Teja Sri	Teja Sri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	K.Sonia	K.Sonia	K.Sonia	K.Sonia	K.Sonia
24.	15UP1A0426	Vijitha	Vijitha	Vijitha	Vijitha	Vijitha
25.	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Hibriti	Hibriti	Hibriti	Hibriti	Hibriti
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana



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Telangana State

33.	15UP1A0436	Vidya	vidya	vidya	vidya	vidya
34.	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
35.	15UP1A0438	Varshini	Varshini	Varshini	Varshini	Varshini
36.	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
40.	15UP1A0403	prassana	prassana	prassana	prassana	prassana


COORDINATOR


ECE, HOD

Head of the Department
Electronics and Communication Engineering
Vignans Institute of Management and Technology for Women
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Email: info.vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

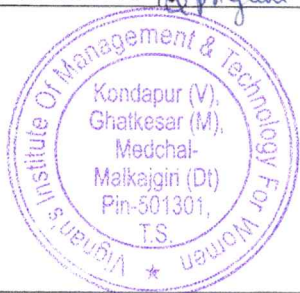
Date: 15-10-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	15-10-18	16-10-18	20-10-18	22-10-18	23-10-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keerthi	Keerthi	Keerthi	Keerthi	Keerthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
7.	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	Sw	Sw	Sw	Sw	Sw
10.	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
11.	15UP1A0451	G.nikitha	G.nikitha	G.nikitha	G.nikitha	G.nikitha
12.	15UP1A0452	Sristha	Sristha	Sristha	Sristha	Sristha
13.	15UP1A0453	Ab	Ab	Ab	Ab	Ab
14.	15UP1A0454	K.Prf	K.Prf	K.Prf	K.Prf	K.Prf
15.	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
16.	15UP1A0456	Sravya	Sravya	Sravya	Sravya	Sravya
17.	15UP1A0457	Harsha	Harsha	Harsha	Harsha	Harsha
18.	15UP1A0458	Narya	Narya	Narya	Narya	Narya
19.	15UP1A0459	Pooj	Pooj	Pooj	Pooj	Pooj
20.	15UP1A0460	Sirija	Sirija	Sirija	Sirija	Sirija
21.	15UP1A0461	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
22.	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
23.	15UP1A0463	H	H	H	H	H
24.	15UP1A0464	Shivapriya	Shivapriya	Shivapriya	Shivapriya	Shivapriya
25.	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
26.	15UP1A0466	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
27.	15UP1A0467	M.Yase	M.Yase	M.Yase	M.Yase	M.Yase
28.	15UP1A0468	Anusha	Anusha	Anusha	Anusha	Anusha
29.	15UP1A0469	Veda	Veda	Veda	Veda	Veda
30.	15UP1A0470	Yash	Yash	Yash	Yash	Yash
31.	15UP1A0472	paitya	paitya	paitya	paitya	paitya
32.	15UP1A0473	Manasa	Manasa	Manasa	Manasa	Manasa
33.	15UP1A0474	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
34.	15UP1A0475	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka



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35.	15UP1A0476	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
36.	15UP1A0477	Kalyani	Kalyani	Kalyani	Kalyani	Kalyani
37.	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
38.	15UP1A0479	Minisha	Minisha	Minisha	Minisha	Minisha
39.	15UP1A0480	Y. Puf	Y. Puf	Y. Puf	Y. Puf	Y. Puf


COORDINATOR


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Head of the Department
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Vignn's Institute of Management and Technology for Women
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

Date: 24-10-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	24-10-18	25-10-18	26-10-18	27-10-18	29-10-18
1.	15UP1A0401	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
2.	15UP1A0402	vaulha	vaulha	vaulha	vaulha	vaulha
3.	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4.	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5.	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6.	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7.	15UP1A0408	Keethi	Keethi	Keethi	Keethi	Keethi
8.	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9.	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10.	15UP1A0411	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
11.	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
12.	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
13.	15UP1A0415	Manika	Manika	Manika	Manika	Manika
14.	15UP1A0416	Devika	Devika	Devika	Devika	Devika
15.	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
16.	15UP1A0418	Hanipriya	Hanipriya	Hanipriya	Hanipriya	Hanipriya
17.	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
18.	15UP1A0420	Tejasri	Tejasri	Tejasri	Tejasri	Tejasri
19.	15UP1A0421	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
20.	15UP1A0422	Uma	Uma	Uma	Uma	Uma
21.	15UP1A0423	Prathyusha	Prathyusha	Prathyusha	Prathyusha	Prathyusha
22.	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
23.	15UP1A0425	K. Sonia	K. Sonia	K. Sonia	K. Sonia	K. Sonia
24.	15UP1A0426	Vidit	Vidit	Vidit	Vidit	Vidit
25.	15UP1A0427	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha
26.	15UP1A0428	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
27.	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
28.	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
29.	15UP1A0431	Lipika	Lipika	Lipika	Lipika	Lipika
30.	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
31.	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya



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32.	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
33.	15UP1A0436	Vidya	vidya	vidya	vidya	vidya
34.	15UP1A0437	Danya	Danya	Danya	Danya	Danya
35.	15UP1A0438	Vaishni	Vaishni	Vaishni	Vaishni	Vaishni
36.	15UP1A0439	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
37.	15UP1A0440	Nandini	Nandini	Nandini	Nandini	Nandini
38.	15UP1A0401	Meghana	Meghana	Meghana	Meghana	Meghana
39.	15UP1A0402	Valsha	Valsha	Valsha	Valsha	Valsha
40.	15UP1A0403	Prasanna	Prasanna	Prasanna	Prasanna	Prasanna


COORDINATOR


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Electronics and Communication Engineering
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Design and FPGA Implementation of DSP Processor using Verilog

Academic Year: 2018-19

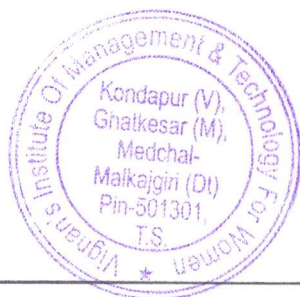
Date: 24-10-2018

B.Tech IV-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	24-10-18	25-10-18	26-10-18	27-10-18	29-10-18
1.	15UP1A0441	Swetha	Swetha	Swetha	Swetha	Swetha
2.	15UP1A0442	Archana	Archana	Archana	Archana	Archana
3.	15UP1A0443	Manasa	Manasa	Manasa	Manasa	Manasa
4.	15UP1A0444	Keelthi	Keelthi	Keelthi	Keelthi	Keelthi
5.	15UP1A0445	Priyanka	Priyanka	Priyanka	Priyanka	Priyanka
6.	15UP1A0446	Mamatha	Mamatha	Mamatha	Mamatha	Mamatha
7.	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
8.	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
9.	15UP1A0449	SN	SN	SN	SN	SN
10.	15UP1A0450	Joshua	Joshua	Joshua	Joshua	Joshua
11.	15UP1A0451	Si-nikitha	Si-nikitha	Si-nikitha	Si-nikitha	Si-nikitha
12.	15UP1A0452	Sinsha	Sinsha	Sinsha	Sinsha	Sinsha
13.	15UP1A0453	AD	AD	AD	AD	AD
14.	15UP1A0454	K.Prf	K.Prf	K.Prf	K.Prf	K.Prf
15.	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
16.	15UP1A0456	Saavya	Saavya	Saavya	Saavya	Saavya
17.	15UP1A0457	Harsha	Harsha	Harsha	Harsha	Harsha
18.	15UP1A0458	Navya	Navya	Navya	Navya	Navya
19.	15UP1A0459	Pooj	Pooj	Pooj	Pooj	Pooj
20.	15UP1A0460	Sirija	Sirija	Sirija	Sirija	Sirija
21.	15UP1A0461	Lavanya	Lavanya	Lavanya	Lavanya	Lavanya
22.	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
23.	15UP1A0463	Sh	Sh	Sh	Sh	Sh
24.	15UP1A0464	shivaPriya	shivaPriya	shivaPriya	shivaPriya	shivaPriya
25.	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
26.	15UP1A0466	Sravanthi	Sravanthi	Sravanthi	Sravanthi	Sravanthi
27.	15UP1A0467	M.Yas	M.Yas	M.Yas	M.Yas	M.Yas
28.	15UP1A0468	Anusha	Anusha	Anusha	Anusha	Anusha
29.	15UP1A0469	Veda	Veda	Veda	Veda	Veda
30.	15UP1A0470	yash	yash	yash	yash	yash
31.	15UP1A0472	paiya	paiya	paiya	paiya	paiya
32.	15UP1A0473	Manasa	Manasa	Manasa	Manasa	Manasa



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Kondapur(V), Ghatkesar(M), Medchal-Malkajgiri(D)-501
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33.	15UP1A0474	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha.
34.	15UP1A0475	S.priyanka	S.priyanka	S.priyanka	S.priyanka	S.priyanka
35.	15UP1A0476	Nikitha	Nikitha	Nikitha	Nikitha	Nikitha.
36.	15UP1A0477	kalyani	kalyani	kalyani	kalyani	kalyani
37.	15UP1A0478	Mahalhe	Mahalhe	Mahalhe	Mahalhe	Mahalhe.
38.	15UP1A0479	Minisha	Minisha	Minisha	Minisha	Minisha
39.	15UP1A0480	y.@f	y.@f	y.@f	y.@f	y.@f


COORDINATOR


ECE, HOD

Head of the Department
Electronics and Communication Engineering
Vignan's Institute of Management and Technology for Women
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Phone: +08615 200006/07/08 Email: info@vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 31-10-2018.

PROGRAM REPORT

Name of the Add on Course: Design and FPGA Implementation of DSP Processor using Verilog

Day/Duration: 35 HOURS

Time: 4:00PM TO 5:00PM

Resource Person: Mr. ArjunModi, Sr.Engineer, Amtronics PVT, LTD, Hyderabad.

Name of the Coordinator: Mr. J. Sunil Kumar, Assistant Professor, VMTW



Number of the Participants: 79

Topics covered: The following topics covered in this program

Course Outcomes: Work with real time projects using Architectural transformation techniques

COs	At the end of the course, students will have the ability to:	POs Mapped	Strength of mapping
CO1	Understand the LTI system characteristics and Multi-rate signal processing.	PO1,PO3	3
CO2	Understand the significance of various filter structures and effects of round off errors	PO1,PO3	2
CO3	Understand the inter-relationship between DFT and various transforms	PO1,PO2	2
CO4	Understand different types of faults that can occur in a system and learn the concept of testing and adding extra hardware to improve testability of system	PO1,PO2	3
CO5	Design building blocks of data path systems, memories and simple logic circuits using PLA, PAL, FPGA and CPLD	PO1,PO2	2

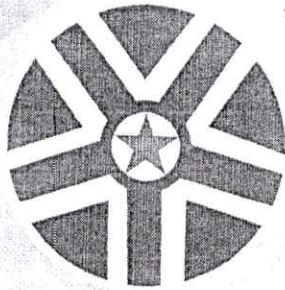
Assessment Procedure: The assessment of the Add on course is conducted in Multiple Choice Questions through offline Mode.

Coordinator




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Kondapur Village, Ghatkesar Mandal, Medchal - Malkajgiri Dist - 501 301 TS, INDIA



Armtronics
Dedicated to Electronics

Certificate of Course Completion

This is to certify that

DHODLA ALEKHYA

has successfully completed the Add-on course on "DESIGN & FPGA IMPLEMENTATION OF DSP PROCESSOR USING VERILOG" held from 11TH SEP to 29TH OCT, 2018, Organized by the Department of Electronics and Communication Engineering.

In association with Amtronics, Hyderabad.



[Signature]
Co-ordinator

[Signature]
HoD, ECE
Head of the Department
Electronics and Communication Engineering
Vignans Institute of Management and Technology for Women
Kondapur (V), Ghatkesar (M), R.R. Dist-501 301

PRINCIPAL
Vignans Institute of Management & Technology For Women
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Telangana State

[Signature]
Principal



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Email: info@vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VMTW/ECE/AOC/2017-18/I/02

Date:15-08-2017

CIRCULAR

This is to inform all the III B. Tech ECE students that there will be an Add on course on "Latest trends in chip design for Area and Power Optimization "in association with AMTRONICS PVT LTD. Hyderabad, from 18-08-2017 to 27-09-2017.All students are invited to take part in this course. The participating students will be honored with certificates of participation. During the course you will be encouraged to interact with the speaker and the other participants through the case study discussions.

HOD

Head of the Department
Electronics and Communication Engineering
Vignan's Institute of Management and Technology for Women
Kondapur (V), Ghatkesar (M), R.R. Dist-501 301

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The Principal, for kind information

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Notice board

III.B.Tech students

Dept. file



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Vignan's Institute of Management & Technology For Women
Kondapur(V),Ghatkesar(M),Medchal-Malkajgiri(Dt)-501301
Telangana State

About the Department:

Department of Electronics and Communication Engineering was started since the inception of Vignan's Institute of Management and Technology for Women during 2008 with an initial intake of 90. The strength was enhanced to 120 during 2010. The Department had added Post graduate programme in VLSI during the year 2011 and Embedded Systems during 2014 with an intake of 18 each.

The Department has state-of-art laboratories equipped with advanced and well maintained equipment, continuously updated application software packages, more than adequate computing systems with 24x7, 30 MBPS internet facility.

About the Course:

VLSI Stands for Very-large-scale integration (VLSI), which creates an integrated circuit (IC) by combining millions of MOS (Metal Oxide Silicon transistor) transistors over a single chip. The microprocessor and memory chips are VLSI (Very-large-scale integration) devices. Before the intro of VLSI technology, most ICs had a limited set of roles they could perform. IC (Integrated Circuits) are used in various types of electronic devices. Our mobile phone consists of IC. IC is a circuit where all or some of the circuit elements are inseparably linked and electrically interconnected, so it's considered indivisible for construction and commerce. Before VLSI, IC size used to be much larger than it is now. Because of VLSI, designers can now add millions of transistors and other components on a tiny chip.

Course Objectives:

- Overview of IC Design
- Aspects of IC Design
- Introduction and Device Characteristics
- Analog IC Design
- Digital IC Design
- Semicustom IC Design/PLD
- Introduction to cadence EDA
- Op Amp Design and Compensation
- VLSI Signal Processing
- VLSI Communication System Design

- Mixed Signal Design /RF IC Design
- FDGA/VHDL

Expected Outcomes:

At the end of Workshop, participants will be able to

- Model digital systems in VHDL and SystemC at different levels of abstraction.
- Partition a digital system into different subsystems.
- Simulate and verify a design.
- Transfer a design from a version possible to simulate to a version possible to synthesize.
- Use computer-aided design tools to synthesize, map, place, routing, and download the digital designs on the FPGAboard.
- Apply knowledge of mathematics, science, and engineering to design and analysis of analog integrated circuits.
- Identify, formulate, and solve engineering problems in the area of analog integrated circuits.
- Use the techniques, skills, and modern programming tools such as Mentor Graphics, necessary for engineering practice.



Resource Person:
Mr. Arjun Modi,
Technical Manager,
Amtronics, Hyderabad.

Co-ordinator:
Mr. G. Narendra,
Assistant Professor, Dept. of ECE,
Contact No: +91 94926 39647

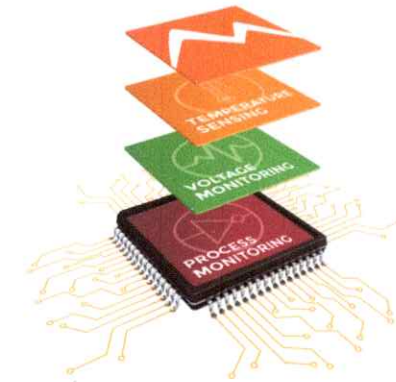
Last Date For Registration: 13th Aug, 2017

VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN

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Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad.

Kondapur (V), Ghatkesar (M), Medchal - Malkajgiri (D) - 501 30



ADD-ON COURSE ON "LATEST TRENDS IN CHIP DESIGN FOR AREA & POWER OPTIMIZATION"

18TH AUG TO 27TH SEP, 2017

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Vignan's Institute of Management & Technology For Women
Kondapur(V), Ghatkesar(M), Medchal-Malkajgiri(Dt) - 501301
Telangana State

Duration of the Course: **35 Hrs**

Venue:
'B'-Block Seminar Hall, VMTW.

Organized By:
**DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING**



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Kondapur (V), Ghatkesar (M), Medchal - Malkajgiri (D) - 501 301 TS INDIA
Phone: +08615 200006/07/08 Email: info@vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 15-08-2017

B.Tech III-I SEM

DAY WISE SCHEDULE SHEET

SECTION: ECE-A&B

Room number: B-BLOCK SEMINAR HALL.

S.NO	DAY	TOPIC	TIMINGS	DURATION
1.	18-Aug-17	Introduction	04:00pm to 05:00pm	1 hour
2.	19-Aug-17	Full-Voltage Scaling, Constant-	04:00pm to 05:00pm	1 hour
3.	21-Aug-17	MOSFET Capacitances,	04:00pm to 05:00pm	1 hour
4.	22-Aug-17	Properties of MOSFETs	04:00pm to 05:00pm	1 hour
5.	23-Aug-17	Challenges of MOSFET Scaling	04:00pm to 05:00pm	1 hour
6.	24-Aug-17	Layout of CMOS Logic	04:00pm to 05:00pm	1 hour
7.	25-Aug-17	Design Rules, Stick	04:00pm to 05:00pm	1 hour
8.	26-Aug-17	Switching Properties of	04:00pm to 05:00pm	1 hour
9.	28-Aug-17	Static and dynamic	04:00pm to 05:00pm	1 hour
10.	29-Aug-17	CMOS Inverter: Basic Circuit	04:00pm to 05:00pm	1 hour
11.	30-Aug-17	CMOS Inverter: Basic Circuit	04:00pm to 05:00pm	1 hour
12.	31-Aug-17	DC Characteristics, Noise	04:00pm to 05:00pm	1 hour
13.	1-Sep-17	considerations,	04:00pm to 05:00pm	1 hour
14.	2-Sep-17	Inverter Switching	04:00pm to 05:00pm	1 hour
15.	4-Sep-17	Static CMOS Logic Elements:	04:00pm to 05:00pm	1 hour
16.	5-Sep-17	EDA tools, architecture design	04:00pm to 05:00pm	1 hour
17.	6-Sep-17	Overview of SOC Design	04:00pm to 05:00pm	1 hour
18.	7-Sep-17	Techniques to improve a specific	04:00pm to 05:00pm	1 hour
19.	8-Sep-17	CMOS Inverter: Basic Circuit	04:00pm to 05:00pm	1 hour
20.	9-Sep-17	DC Characteristics, Noise	04:00pm to 05:00pm	1 hour
21.	11-Sep-17	Platforms and SoC Design,	04:00pm to 05:00pm	1 hour
22.	12-Sep-17	, Designing Communication	04:00pm to 05:00pm	1 hour
23.	13-Sep-17	CMOS Inverter: Basic Circuit	04:00pm to 05:00pm	1 hour
24.	14-Sep-17	DC Characteristics, Noise	04:00pm to 05:00pm	1 hour
25.	15-Sep-17	SOC Design and Test	04:00pm to 05:00pm	1 hour
26.	16-Sep-17	Design methodologies for SoC	04:00pm to 05:00pm	1 hour
27.	18-Sep-17	Noise and signal integrity	04:00pm to 05:00pm	1 hour
28.	19-Sep-17	System Integration issues for	04:00pm to 05:00pm	1 hour
29.	20-Sep-17	SoC Test Scheduling and Test	04:00pm to 05:00pm	1 hour
30.	21-Sep-17	System Level Power Estimation	04:00pm to 05:00pm	1 hour



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31.	22-Sep-17	Transaction Level Modeling	04:00pm to 05:00pm	1 hour
32.	23-Sep-17	Design Space,Exploration,	04:00pm to 05:00pm	1 hour
33.	25-Sep-17	SoC Test Scheduling and Test	04:00pm to 05:00pm	1 hour
34.	26-Sep-17	SoC TestResource partition	04:00pm to 05:00pm	1 hour
35.	27-Sep-17	Test conducted & Feedback	04:00pm to 05:00pm	1 hour
Total 35 hours				

Narender
COORDINATOR



[Signature]

HOD

Head of the Department
Electronics and Communication Engineering
Vignans Institute of Management and Technology for Women
Kondapur (V), Ghatkesar (M), R.R. Dist-501 301

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Phone: +08615 200006/07/08 Email: info@vmtw.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year: 2017-18

Date: 11-08-2017

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

B.Tech III-I SEM STUDENT REGISTRATION FORM SECTION: ECE-A

S.NO	ROLL NUMBER	NAME OF THE STUDENT	SIGNATURE
1	15UP1A0401	BEDUDHURI MEGHANA	Meghana
2	15UP1A0402	C VARSHA REDDY	Varsha
3	15UP1A0403	CHENNU LAXMI PRASANNA	Laxmi
4	15UP1A0405	CHILUMULA RACHANA	Rachana
5	15UP1A0406	CHUNCHU RAMYA SRI	Ramyasri
6	15UP1A0407	DADI SHIVANJALI	Anjali
7	15UP1A0408	DEVARAKONDA KEERTHI	Keerthi
8	15UP1A0409	DEVARAKONDA PREETHI	Preethi
9	15UP1A0410	DHODLA ALEKHYA	Alekhyasri
10	15UP1A0411	DUMALA PRIYANKA	Priyanka
11	15UP1A0412	G VYSHNAVI	Vyshnavi
12	15UP1A0413	GADDAMEEDI ANUSHA	Anusha
13	15UP1A0414	GANGAPURAM HIMAJA	Himaja
14	15UP1A0415	GOPALADAS MOUNIKA	Mounika
15	15UP1A0416	GUNDA DEVIKA	Devika
16	15UP1A0417	GUNTI SRAVANI	Sravani
17	15UP1A0418	HARIVENKATANAGA HARIPRIYA	Haripriya
18	15UP1A0419	JAKKIDI PRANAYA	Pranaya
19	15UP1A0420	KAKANI TEJA SRI	Tejasri
20	15UP1A0421	KANDADI NIKHITHA	Nikhitha
21	15UP1A0422	KANDHATI UMA	Uma
22	15UP1A0423	KETHIREDDY PRATHYUSHA	Prathyusha
23	15UP1A0424	KODEMALA SAIKRUPA	Sai Krupa
24	15UP1A0425	KOLA SONIA	K. Sonia
25	15UP1A0426	L VIJITHA	Vijitha
26	15UP1A0427	MAINELLY NIKHITHA	Nikhitha
27	15UP1A0428	MALLELA MAMATHA	Mamatha
28	15UP1A0429	MATTI PALLAVI	Pallavi
29	15UP1A0430	MOJJA KAVERI	Kaveri
30	15UP1A0431	MULLAPUDI VENKATA LIKHITA	Likhita
31	15UP1A0432	PABBA VIKASINI	Vikasini
32	15UP1A0434	PALADUGULA SRIKAVYA	Kavya
33	15UP1A0435	PAPINENI BHAVANA	Bhavana
34	15UP1A0436	PERUGUPALLI VIDYULLEKHA	Vidhyullekha




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Telangana State

35	15UP1A0437	PINNAPU REDDY RAMYA	Ramya
36	15UP1A0438	S AMRUTHA VARSHINI	Varshini
37	15UP1A0439	SALLA VARSHINI	Varshini
38	15UP1A0440	SAMUDRALA NANDINI	
39	15UP1A0441	SUDAGANI SWETHA	Swetha
40	15UP1A0442	VONTARI ARCHANA	Archana

Naindra
COORDINATOR

Ho
HOD

Head of the Department
Electronics and Communication Engineering
Vignn's Institute of Management & Technology For Women
Kondapur (V), Ghatkesar (M), Medchal-Malkajgiri (Dt) - 501301
T.S.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year: 2017-18

Date: 17-08-2017

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

B.Tech III-I SEM STUDENT REGISTERED LIST SECTION: ECE-A

S.NO	ROLL NUMBER	NAME OF THE STUDENT
1	15UP1A0401	BEDUDHURI MEGHANA
2	15UP1A0402	C VARSHA REDDY
3	15UP1A0403	CHENNU LAXMI PRASANNA
4	15UP1A0405	CHILUMULA RACHANA
5	15UP1A0406	CHUNCHU RAMYA SRI
6	15UP1A0407	DADI SHIVANJALI
7	15UP1A0408	DEVARAKONDA KEERTHI
8	15UP1A0409	DEVARAKONDA PREETHI
9	15UP1A0410	DHODLA ALEKHYA
10	15UP1A0412	G VYSHNAVI
11	15UP1A0414	GANGAPURAM HIMAJA
12	15UP1A0415	GOPALADAS MOUNIKA
13	15UP1A0416	GUNDA DEVIKA
14	15UP1A0417	GUNTI SRAVANI
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17	15UP1A0420	KAKANI TEJA SRI
18	15UP1A0421	KANDADI NIKHITHA
19	15UP1A0422	KANDHATI UMA
20	15UP1A0423	KETHIREDDY PRATHYUSHA
21	15UP1A0424	KODEMALA SAIKRUPA
22	15UP1A0425	KOLA SONIA
23	15UP1A0426	L VIJITHA
24	15UP1A0427	MAINELLY NIKHITHA
25	15UP1A0429	MATTI PALLAVI
26	15UP1A0430	MOJJA KAVERI
27	15UP1A0431	MULLAPUDI VENKATA LIKHITA
28	15UP1A0432	PABBA VIKASINI
29	15UP1A0434	PALADUGULA SRIKAVYA
30	15UP1A0435	PAPINENI BHAVANA
31	15UP1A0436	PERUGUPALLI VIDYULLEKHA
32	15UP1A0437	PINNAPU REDDY RAMYA
33	15UP1A0438	S AMRUTHA VARSHINI
34	15UP1A0439	SALLA VARSHINI
35	15UP1A0441	SUDAGANI SWETHA
36	15UP1A0442	VONTARI ARCHANA

Varudha
COORDINATOR

[Signature]
HOD



[Signature]
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Head of the Department
Electronics and Communication Engineering
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year: 2017-18

Date: 11-08-2017

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

B.Tech III-I SEM

STUDENT REGISTRATION FORM SECTION: ECE-B

S.NO	ROLL NUMBER	NAME OF THE STUDENT	SIGNATURE
1	15UP1A0443	A MANASA REDDY BODELA	Manasa
2	15UP1A0444	BALA THARUNA KEERTHI	Bala
3	15UP1A0445	BANALA PRIYANKA	Priyanka
4	15UP1A0446	BANGARAM MAMATHA	Mamatha
5	15UP1A0447	BASIREDDY BHARATHI REDDY	Bharathi
6	15UP1A0448	BILLAKANTI RAVALI	Ravali
7	15UP1A0449	DEEKONDA SUGANDHA	Sugandha
8	15UP1A0450	GADDAM JOSHNA	Joshna
9	15UP1A0451	GOGINENI NIKITHA	Nikitha
10	15UP1A0452	GUNDAGANI NAGASHIRISHA	Nagashirisha
11	15UP1A0453	JALA MOUNIKA	Mounika
12	15UP1A0454	K RAMYA REDDY	Ramya
13	15UP1A0455	KANALA KAVYA REDDY	Kavya
14	15UP1A0456	KANDUKURI SRAVYA	Sravya
15	15UP1A0457	KARNATI SRIHARSHA	Sriharsha
16	15UP1A0458	KASULA NAVYA SRI	Navya
17	15UP1A0459	KETHIREDDY RAMYA	Ramya
18	15UP1A0460	KOMATIREDDY SIRIJA	Sirija
19	15UP1A0461	LAVANYA SEELAM	Seelam
20	15UP1A0462	M HARICHANDANA	Chandana
21	15UP1A0463	MAHAJAN SRADHA	Sradha
22	15UP1A0464	MANCHALA SHIVAPRIYA	Shivapriya
23	15UP1A0465	MANTIPALLY PRAVALIKA	Pravalika
24	15UP1A0466	METTU SRAVANTHI	Sravanthi
25	15UP1A0467	MUNAGALA YASHASWINI	Yashaswini
26	15UP1A0468	NAGANOLLU ANUSHA REDDY	Anusha
27	15UP1A0469	PACHA VEDASRI	Vedasri
28	15UP1A0470	VENKATA YASHASWINI	Yashaswini
29	15UP1A0471	PERAMALLA KAVYA	Kavya
30	15UP1A0472	POCHAMPALLY PRIYANKA	Priyanka
31	15UP1A0473	POTHEPAKA MANASA	Manasa
32	15UP1A0474	SHEELA NIKITHA	Sheela
33	15UP1A0475	SHERIKAR PRIYANKA	Priyanka
34	15UP1A0476	SHIVA NIKHITHA	Nikhitha




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35	15UP1A0477	SUNKI KALYANI	<i>do</i>
36	15UP1A0478	VEMURI MAHATHI	<i>Mahathi</i>
37	15UP1A0479	YASA MINISHA REDDY	<i>Y. Divya</i>
38	15UP1A0480	YERUVA SAGAR BALA DIVYA	<i>Divya</i>
39	16UP5A0401	K.DIVYA	<i>Divya</i>
40	15C31A0432	GADILA PRASANNA LAXMI	<i>A</i>

Nandya
COORDINATOR

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Academic Year: 2017-18

Date: 17-08-2017

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B.Tech III-I SEM

STUDENT REGISTERED LIST

SECTION: ECE-B

S.NO	ROLL NUMBER	NAME OF THE STUDENT
1	15UP1A0443	A MANASA REDDY BODELA
2	15UP1A0444	BALA THARUNA KEERTHI
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4	15UP1A0447	BASIREDDY BHARATHI REDDY
5	15UP1A0448	BILLAKANTI RAVALI
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20	15UP1A0464	MANCHALA SHIVAPRIYA
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23	15UP1A0467	MUNAGALA YASHASWINI
24	15UP1A0468	NAGANOLLU ANUSHA REDDY
25	15UP1A0471	PERAMALLA KAVYA
26	15UP1A0472	POCHAMPALLY PRIYANKA
27	15UP1A0473	POTHEPAKA MANASA
28	15UP1A0474	SHEELA NIKITHA
29	15UP1A0475	SHERIKAR PRIYANKA
30	15UP1A0476	SHIVA NIKHITHA
31	15UP1A0477	SUNKI KALYANI
32	15UP1A0478	VEMURI MAHATHI
33	15UP1A0480	YERUVA SAGAR BALA DIVYA
34	16UP5A0401	K.DIVYA
35	15C31A0432	GADILA PRASANNA LAXMI

A. Aravinda
COORDINATOR

kb
HOD



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PRINCIPAL
Head of the Department
Electronics and Communication Engineering
Vignan's Institute of Management & Technology For Women
Kondapur (V), Ghatkesar (M), Medchal-Malkajgiri (Dt)-501301
Vignan's Institute of Management & Technology For Women
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 18-08-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll Number	18-Aug-17	19-Aug-17	21-Aug-17	22-Aug-17	23-Aug-17
1	15UP1A0401	Maya	Maya	Maya	Maya	Maya
2	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Ruhana	Ruhana	Ruhana	Ruhana	Ruhana
5	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	Kt	Kt	Kt	Kt	Kt
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhyaa	Alekhyaa	Alekhyaa	Alekhyaa	Alekhyaa
10	15UP1A0412	Vyshaani	Vyshaani	Vyshaani	Vyshaani	Vyshaani
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Manika	Manika	Manika	Manika	Manika
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
15	15UP1A0418	hasipriya	hasipriya	hasipriya	hasipriya	hasipriya
16	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
17	15UP1A0420	Tejasri	Tejasri	Tejasri	Tejasri	Tejasri
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	lmsa	lmsa	lmsa	lmsa	lmsa
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	k.sonia	k.sonia	k.sonia	k.sonia	k.sonia
23	15UP1A0426	Vijetha	Vijetha	Vijetha	Vijetha	Vijetha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Likanti	Likanti	Likanti	Likanti	Likanti
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
31	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
32	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
33	15UP1A0438	Vaishali	Vaishali	Vaishali	Vaishali	Vaishali
34	15UP1A0439	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 18-08-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll Number	18-Aug-17	19-Aug-17	21-Aug-17	22-Aug-17	23-Aug-17
1	15UP1A0443	Man	Man	Man	Man	Man
2	15UP1A0444	Keer	Keer	Keer	Keer	Keer
3	15UP1A0445	Priya	Priya	Priya	Priya	Priya
4	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
5	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UP1A0449	Sua	Sua	Sua	Sua	Sua
7	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UP1A0451	G. Nikitha	G. Nikitha	G. Nikitha	G. Nikitha	G. Nikitha
9	15UP1A0452	C	C	C	C	C
10	15UP1A0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UP1A0454	K. Ruj	K. Ruj	K. Ruj	K. Ruj	K. Ruj
12	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
13	15UP1A0456	S	S	S	S	S
14	15UP1A0457	S	S	S	S	S
15	15UP1A0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UP1A0460	Sija	Sija	Sija	Sija	Sija
17	15UP1A0461	S	S	S	S	S
18	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UP1A0463	S	S	S	S	S
20	15UP1A0464	Shiba	Shiba	Shiba	Shiba	Shiba
21	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
22	15UP1A0466	S	S	S	S	S
23	15UP1A0467	S	S	S	S	S
24	15UP1A0468	S	S	S	S	S
25	15UP1A0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UP1A0472	Priya	Priya	Priya	Priya	Priya
27	15UP1A0473	Manu	Manu	Manu	Manu	Manu
28	15UP1A0474	Deep	Deep	Deep	Deep	Deep
29	15UP1A0475	D. Priyanka	D. Priyanka	D. Priyanka	D. Priyanka	D. Priyanka
30	15UP1A0476	N	N	N	N	N
31	15UP1A0477	S	S	S	S	S
32	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
33	15UP1A0480	Y. Ruj	Y. Ruj	Y. Ruj	Y. Ruj	Y. Ruj
34	16UP5A0401	Ruja	Ruja	Ruja	Ruja	Ruja
35	15C31A0432	P	P	P	P	P

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 24-08-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

.No	Roll Number	24-Aug-17	25-Aug-17	26-Aug-17	28-Aug-17	29-Aug-17
1	15UP1A0401	Mel	Mel	Mel	Mel	Mel
2	15UP1A0402	Vaisha	Vaisha	Vaisha	Vaisha	Vaisha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	H	H	H	H	H
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10	15UP1A0412	Vishwanth	Vishwanth	Vishwanth	Vishwanth	Vishwanth
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Mounika	Mounika	Mounika	Mounika	Mounika
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Shravani	Shravani	Shravani	Shravani	Shravani
15	15UP1A0418	Haseipriya	Haseipriya	Haseipriya	Haseipriya	Haseipriya
16	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
17	15UP1A0420	Teja Sri	Tejasri	Teja Sri	Tejasri	Teja Sri
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	Elma	Elma	Elma	Elma	Elma
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	k. Sonia	k. Sonia	k. Sonia	k. Sonia	k. Sonia
23	15UP1A0426	Vijetha	Vijetha	Vijetha	Vijetha	Vijetha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Likhitha	Likhitha	Likhitha	Likhitha	Likhitha
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bharana	Bharana	Bharana	Bharana	Bharana
31	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
32	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
33	15UP1A0438	Vaishvi	Vaishvi	Vaishvi	Vaishvi	Vaishvi
34	15UP1A0439	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 24-08-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll Number	24-Aug-17	25-Aug-17	26-Aug-17	28-Aug-17	29-Aug-17
1	15UP1A0443	Maha	Maha	Maha	Maha	Maha
2	15UP1A0444	Keo	Keo	Keo	Keo	Keo
3	15UP1A0445	Priya	Priya	Priya	Priya	Priya
4	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
5	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UP1A0449	Sua	Sua	Sua	Sua	Sua
7	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UP1A0451	G. Nithitha	G. Nithitha	G. Nithitha	G. Nithitha	G. Nithitha
9	15UP1A0452	Ch	Ch	Ch	Ch	Ch
10	15UP1A0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UP1A0454	K. Puf	K. Puf	K. Puf	K. Puf	K. Puf
12	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
13	15UP1A0456	Sray	Sray	Sray	Sray	Sray
14	15UP1A0457	Se	Se	Se	Se	Se
15	15UP1A0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UP1A0460	Sriya	Sriya	Sriya	Sriya	Sriya
17	15UP1A0461	S	S	S	S	S
18	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UP1A0463	Shi	Shi	Shi	Shi	Shi
20	15UP1A0464	Shika	Shika	Shika	Shika	Shika
21	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
22	15UP1A0466	Sray	Sray	Sray	Sray	Sray
23	15UP1A0467	AB				
24	15UP1A0468	As	As	As	As	As
25	15UP1A0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UP1A0472	Purk	Purk	Purk	Purk	Purk
27	15UP1A0473	Mans	Mans	Mans	Mans	Mans
28	15UP1A0474	Om	Om	Om	Om	Om
29	15UP1A0475	P. Priyanka	P. Priyanka	P. Priyanka	P. Priyanka	P. Priyanka
30	15UP1A0476	Nuf	Nuf	Nuf	Nuf	Nuf
31	15UP1A0477	Lo	Lo	Lo	Lo	Lo
32	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
33	15UP1A0480	Y. Puf	Y. Puf	Y. Puf	Y. Puf	Y. Puf
34	16UP5A0401	Diya	Diya	Diya	Diya	Diya
35	15C31A0432	Ph	Ph	Ph	Ph	Ph

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

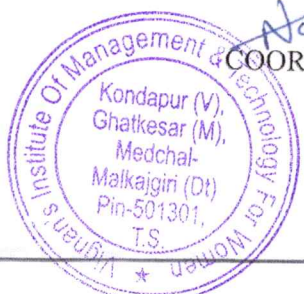
Date: 30-08-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll number	30-Aug-17	31-Aug-17	1-Sep-17	2-Sep-17	4-Sep-17
1	15UP1A0401	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
2	15UP1A0402	Vaasha	Vaasha	Vaasha	Vaasha	Vaasha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Manika	Manika	Manika	Manika	Manika
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
15	15UP1A0418	Hasepriya	Hasepriya	Hasepriya	Hasepriya	Hasepriya
16	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
17	15UP1A0420	Tejasri	Tejasri	Tejasri	Tejasri	Tejasri
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	Alma	Alma	Alma	Alma	Alma
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	k.sonia	k.sonia	k.sonia	k.sonia	k.sonia
23	15UP1A0426	Vijitha	Vijitha	Vijitha	Vijitha	Vijitha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Likhitha	Likhitha	Likhitha	Likhitha	Likhitha
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
31	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
32	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
33	15UP1A0438	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
34	15UP1A0439	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 30-08-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll number	30-Aug-17	31-Aug-17	1-Sep-17	2-Sep-17	4-Sep-17
1	15UP1A0443	Mani	Mani	Mani	Mani	Mani
2	15UP1A0444	Keb	Keb	Keb	Keb	Keb
3	15UP1A0445	Priya	Priya	Priya	Priya	Priya
4	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
5	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UP1A0449	Srua	Srua	Srua	Srua	Srua
7	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UP1A0451	G.nikittha	G.nikittha	G.nikittha	G.nikittha	G.nikittha
9	15UP1A0452	Ce	Ce	Ce	AB	Ce
10	15UP1A0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UP1A0454	K.Ruf	K.Ruf	K.Ruf	K.Ruf	K.Ruf
12	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
13	15UP1A0456	Sravya	Sravya	Sravya	Sravya	Sravya
14	15UP1A0457	Se	Se	Se	Se	Se
15	15UP1A0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UP1A0460	Srinija	Srinija	Srinija	Srinija	Srinija
17	15UP1A0461	S	S	S	S	S
18	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UP1A0463	Soni	Soni	Soni	Soni	Soni
20	15UP1A0464	Shiba	Shiba	Shiba	Shiba	Shiba
21	15UP1A0465	Pavali	Pavali	Pavali	Pavali	Pavali
22	15UP1A0466	Srav	Srav	Srav	Srav	Srav
23	15UP1A0467	Devi	Devi	Devi	Devi	Devi
24	15UP1A0468	Devi	Devi	Devi	Devi	Devi
25	15UP1A0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UP1A0472	Prith	Prith	Prith	Prith	Prith
27	15UP1A0473	Manu	Manu	Manu	Manu	Manu
28	15UP1A0474	Manu	Manu	Manu	Manu	Manu
29	15UP1A0475	S.priyanka	S.priyanka	S.priyanka	S.priyanka	S.priyanka
30	15UP1A0476	Nay	Nay	Nay	Nay	Nay
31	15UP1A0477	Ko	Ko	Ko	Ko	Ko
32	15UP1A0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
33	15UP1A0480	V.Ruf	V.Ruf	V.Ruf	V.Ruf	V.Ruf
34	16UP5A0401	Diya	Diya	Diya	Diya	Diya
35	15C31A0432	AB	AB	AB	AB	AB

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ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 05-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll Number	5-Sep-17	6-Sep-17	7-Sep-17	8-Sep-17	09-Sep-17
1	15UP1A0401	Mel	Mel	Mel	Mel	Mel
2	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5	15UP1A0406	Ranya	Ranya	Ranya	Ranya	Ranya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	H	H	H	H	H
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhy	Alekhy	Alekhy	Alekhy	Alekhy
10	15UP1A0412	Vishnu	Vishnu	Vishnu	Vishnu	Vishnu
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Manika	Manika	Manika	Manika	Manika
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
15	15UP1A0418	Harpriya	Harpriya	Harpriya	Harpriya	Harpriya
16	15UP1A0419	Pranya	Pranya	Pranya	Pranya	Pranya
17	15UP1A0420	Teja Sri	Teja Sri	Teja Sri	Teja Sri	Teja Sri
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	Uma	Uma	Uma	Uma	Uma
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	K. Sonia	K. Sonia	K. Sonia	K. Sonia	K. Sonia
23	15UP1A0426	Vijitha	Vijitha	Vijitha	Vijitha	Vijitha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Hikmat	Hikmat	Hikmat	Hikmat	Hikmat
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
31	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
32	15UP1A0437	Ranya	Ranya	Ranya	Ranya	Ranya
33	15UP1A0438	Varshini	Varshini	Varshini	Varshini	Varshini
34	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 05-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll Number	5-Sep-17	6-Sep-17	7-Sep-17	8-Sep-17	09-Sep-17
1	15UP1A0443	Mana	Mana	Mana	Mana	Mana
2	15UP1A0444	Kee	Kee	Kee	Kee	Kee
3	15UP1A0445	Priya	Priya	Priya	Priya	Priya
4	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
5	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UP1A0449	Sua	Sua	Sua	Sua	Sua
7	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UP1A0451	G.nikitha	G.nikitha	G.nikitha	G.nikitha	G.nikitha
9	15UP1A0452	Ce	Ce	Ce	AB	Ce
10	15UP1A0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UP1A0454	K. Ruj	K. Ruj	K. Ruj	K. Ruj	K. Ruj
12	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
13	15UP1A0456	Shravya	Shravya	Shravya	Shravya	Shravya
14	15UP1A0457	So	So	So	So	So
15	15UP1A0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UP1A0460	Sriya	Sriya	Sriya	Sriya	Sriya
17	15UP1A0461	S	S	S	S	S
18	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UP1A0463	Shila	Shila	Shila	Shila	Shila
20	15UP1A0464	Shila	Shila	Shila	Shila	Shila
21	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
22	15UP1A0466	Sravya	Sravya	Sravya	Sravya	Sravya
23	15UP1A0467	Ch	Ch	Ch	Ch	Ch
24	15UP1A0468	Abh	Abh	Abh	Abh	Abh
25	15UP1A0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UP1A0472	Prithi	Prithi	Prithi	Prithi	Prithi
27	15UP1A0473	Manas	Manas	Manas	Manas	Manas
28	15UP1A0474	Divy	Divy	Divy	Divy	Divy
29	15UP1A0475	S.priyanka	S.priyanka	S.priyanka	S.priyanka	S.priyanka
30	15UP1A0476	Nitya	Nitya	Nitya	Nitya	Nitya
31	15UP1A0477	Ke	Ke	Ke	Ke	Ke
32	15UP1A0478	AB	Mahathi	Mahathi	Mahathi	Mahathi
33	15UP1A0480	Y. Ruj	Y. Ruj	Y. Ruj	Y. Ruj	Y. Ruj
34	16UP5A0401	Diya	Diya	Diya	Diya	Diya
35	15C31A0432	P	P	P	P	P

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 11-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll Number	11-Sep-17	12-Sep-17	13-Sep-17	14-Sep-17	15-Sep-17
1	15UP1A0401	MDY	MDY	MDY	MDY	MDY
2	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	R	R	R	R	R
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhya	Alekhya	Alekhya	Alekhya	Alekhya
10	15UP1A0412	Vishuani	Vishuani	Vishuani	Vishuani	Vishuani
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Manika	Manika	Manika	Manika	Manika
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
15	15UP1A0418	Hasepriya	Hasepriya	Hasepriya	Hasepriya	Hasepriya
16	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
17	15UP1A0420	Tejasi	Tejasi	Tejasi	Tejasi	Tejasi
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	Ilma	Ilma	Ilma	Ilma	Ilma
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	K.Sonia	K.Sonia	K.Sonia	K.Sonia	K.Sonia
23	15UP1A0426	Vijitha	Vijitha	Vijitha	Vijitha	Vijitha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Palavi	Palavi	Palavi	Palavi	Palavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Hikant	Hikant	Hikant	Hikant	Hikant
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
31	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
32	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
33	15UP1A0438	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
34	15UP1A0439	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana

A. Arundha
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A. Arundha
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 11-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll Number	11-Sep-17	12-Sep-17	13-Sep-17	14-Sep-17	15-Sep-17
1	15UP1A0443	Atana	Atana	Atana	Atana	Atana
2	15UP1A0444	Keo	Keo	Keo	Keo	Keo
3	15UP1A0445	Priya	Priya	Priya	Priya	Priya
4	15UP1A0447	Isharathi	Isharathi	Isharathi	Isharathi	Isharathi
5	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UP1A0449	Suwa	Suwa	Suwa	Suwa	Suwa
7	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UP1A0451	G.nikitha	G.nikitha	G.nikitha	G.nikitha	G.nikitha
9	15UP1A0452	C	C	C	C	C
10	15UP1A0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UP1A0454	K.Rul	K.Rul	K.Rul	K.Rul	K.Rul
12	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
13	15UP1A0456	Shravya	Shravya	Shravya	Shravya	Shravya
14	15UP1A0457	So	So	So	So	So
15	15UP1A0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UP1A0460	Srija	Srija	Srija	Srija	Srija
17	15UP1A0461	S	S	S	S	A
18	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UP1A0463	Shilpa	Shilpa	Shilpa	Shilpa	Shilpa
20	15UP1A0464	Shila	Shila	Shila	Shila	Shila
21	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
22	15UP1A0466	Srav	Srav	Srav	Srav	Srav
23	15UP1A0467	U	U	U	U	U
24	15UP1A0468	U	U	U	U	U
25	15UP1A0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UP1A0472	Priya	Priya	Priya	Priya	Priya
27	15UP1A0473	Mans	Mans	Mans	Mans	Mans
28	15UP1A0474	Any	Any	Any	Any	Any
29	15UP1A0475	S.priyanka	S.priyanka	S.priyanka	S.priyanka	S.priyanka
30	15UP1A0476	Nul	Nul	Nul	Nul	Nul
31	15UP1A0477	Lo	Lo	Lo	Lo	Lo
32	15UP1A0478	mahathi	mahathi	mahathi	mahathi	mahathi
33	15UP1A0480	V.Rul	V.Rul	V.Rul	V.Rul	V.Rul
34	16UP5A0401	Riya	Riya	Riya	Riya	Riya
35	15C31A0432	R	R	R	R	R

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 16-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

.No	Roll Number	16-Sep-17	18-Sep-17	19-Sep-17	20-Sep-17	21-Sep-17
1	15UP1A0401	Mey	Mey	Mey	Mey	Mey
2	15UP1A0402	Varsha	Varsha	Varsha	Varsha	Varsha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5	15UP1A0406	Ramya	Ramya	Ramya	Ramya	Ramya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	Rt	Rt	Rt	Rt	Rt
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhyas	Alekhyas	Alekhyas	Alekhyas	Alekhyas
10	15UP1A0412	Vyshudis	Vyshudis	Vyshudis	Vyshudis	Vyshudis
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Moronica	Moronica	Moronica	Moronica	Moronica
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
15	15UP1A0418	Haseipriya	Haseipriya	Haseipriya	Haseipriya	Haseipriya
16	15UP1A0419	Pranaya	Pranaya	Pranaya	Pranaya	Pranaya
17	15UP1A0420	Teja Sri	Teja Sri	Teja Sri	Teja Sri	Teja Sri
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	Ilma	Ilma	Ilma	Ilma	Ilma
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	K. Sonia	K. Sonia	K. Sonia	K. Sonia	K. Sonia
23	15UP1A0426	Vijitha	Vijitha	Vijitha	Vijitha	Vijitha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Likshitha	Likshitha	Likshitha	Likshitha	Likshitha
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
31	15UP1A0436	Vidhya	Vidhya	Vidhya	Vidhya	Vidhya
32	15UP1A0437	Ramya	Ramya	Ramya	Ramya	Ramya
33	15UP1A0438	Varshini	Varshini	Varshini	Varshini	Varshini
34	15UP1A0439	Varshini	Varshini	Varshini	Varshini	Varshini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana

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PRINCIPAL Head of the Department
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ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 16-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll Number	16-Sep-17	18-Sep-17	19-Sep-17	20-Sep-17	21-Sep-17
1	15UP1A0443	Para	Para	Para	Para	Para
2	15UP1A0444	Keo	Keo	Keo	Keo	Keo
3	15UP1A0445	Riya	Riya	Riya	Riya	Riya
4	15UP1A0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
5	15UP1A0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UP1A0449	Sua	Sua	Sua	Sua	Sua
7	15UP1A0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UP1A0451	G.Nikittha	G.Nikittha	G.Nikittha	G.Nikittha	G.Nikittha
9	15UP1A0452	C	C	C	C	C
10	15UP1A0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UP1A0454	K.Ruf	K.Ruf	K.Ruf	K.Ruf	K.Ruf
12	15UP1A0455	Kavya	Kavya	Kavya	Kavya	Kavya
13	15UP1A0456	Sa	Sa	Sa	Sa	Sa
14	15UP1A0457	Sa	Sa	Sa	Sa	Sa
15	15UP1A0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UP1A0460	Sriya	Sriya	Sriya	Sriya	Sriya
17	15UP1A0461	S	S	S	S	S
18	15UP1A0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UP1A0463	Shila	Shila	Shila	Shila	Shila
20	15UP1A0464	Shila	Shila	Shila	Shila	Shila
21	15UP1A0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
22	15UP1A0466	Sravya	Sravya	Sravya	Sravya	Sravya
23	15UP1A0467	Sravya	Sravya	Sravya	Sravya	Sravya
24	15UP1A0468	Sravya	Sravya	Sravya	Sravya	Sravya
25	15UP1A0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UP1A0472	Priya	Priya	Priya	Priya	Priya
27	15UP1A0473	Mansi	Mansi	Mansi	Mansi	Mansi
28	15UP1A0474	Mansi	Mansi	Mansi	Mansi	Mansi
29	15UP1A0475	S.Priyanka	S.Priyanka	S.Priyanka	S.Priyanka	S.Priyanka
30	15UP1A0476	Mansi	Mansi	Mansi	Mansi	Mansi
31	15UP1A0477	De	De	De	De	De
32	15UP1A0478	Mahathi	Mahathi	Mahathi	AB	Mahathi
33	15UP1A0480	Y.ert	Y.ert	Y.ert	Y.ert	Y.ert
34	16UP5A0401	Riya	Riya	Riya	Riya	Riya
35	15C31A0432	Ra	Ra	Ra	Ra	Ra

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 22-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-A

S.No	Roll Number	22-Sep-17	23-Sep-17	25-Sep-17	26-Sep-17	27-Sep-17
1	15UP1A0401	Mof	Mof	Mof	Mof	Mof
2	15UP1A0402	Vareha	Vareha	Vareha	Vareha	Vareha
3	15UP1A0403	Laxmi	Laxmi	Laxmi	Laxmi	Laxmi
4	15UP1A0405	Rachana	Rachana	Rachana	Rachana	Rachana
5	15UP1A0406	Ranya	Ranya	Ranya	Ranya	Ranya
6	15UP1A0407	Anjali	Anjali	Anjali	Anjali	Anjali
7	15UP1A0408	R	R	R	R	R
8	15UP1A0409	Preethi	Preethi	Preethi	Preethi	Preethi
9	15UP1A0410	Alekhya	Alekhya	Alekhya	Alekhya	Alekhya
10	15UP1A0412	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi	Vyshnavi
11	15UP1A0414	Himaja	Himaja	Himaja	Himaja	Himaja
12	15UP1A0415	Manika	Manika	Manika	Manika	Manika
13	15UP1A0416	Devika	Devika	Devika	Devika	Devika
14	15UP1A0417	Sravani	Sravani	Sravani	Sravani	Sravani
15	15UP1A0418	Hasepriya	Hasepriya	Hasepriya	Hasepriya	Hasepriya
16	15UP1A0419	Pranya	Pranya	Pranya	Pranya	Pranya
17	15UP1A0420	Teja Sri	Teja Sri	Teja Sri	Teja Sri	Teja Sri
18	15UP1A0421	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
19	15UP1A0422	Ilme	Ilme	Ilme	Ilme	Ilme
20	15UP1A0423	Pooj	Pooj	Pooj	Pooj	Pooj
21	15UP1A0424	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa	Sai Krupa
22	15UP1A0425	K.Sonia	K.Sonia	K.Sonia	K.Sonia	K.Sonia
23	15UP1A0426	Vijetha	Vijetha	Vijetha	Vijetha	Vijetha
24	15UP1A0427	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
25	15UP1A0429	Pallavi	Pallavi	Pallavi	Pallavi	Pallavi
26	15UP1A0430	Kaveri	Kaveri	Kaveri	Kaveri	Kaveri
27	15UP1A0431	Nikhitha	Nikhitha	Nikhitha	Nikhitha	Nikhitha
28	15UP1A0432	Vikasini	Vikasini	Vikasini	Vikasini	Vikasini
29	15UP1A0434	Kavya	Kavya	Kavya	Kavya	Kavya
30	15UP1A0435	Bhavana	Bhavana	Bhavana	Bhavana	Bhavana
31	15UP1A0436	Vidya	Vidya	Vidya	Vidya	Vidya
32	15UP1A0437	Ranya	Ranya	Ranya	Ranya	Ranya
33	15UP1A0438	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
34	15UP1A0439	Vaishini	Vaishini	Vaishini	Vaishini	Vaishini
35	15UP1A0441	Sweetha	Sweetha	Sweetha	Sweetha	Sweetha
36	15UP1A0442	Archana	Archana	Archana	Archana	Archana



Narandya
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PRINCIPAL

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ADD ON COURSE NAME: Latest trends in chip design for Area and Power Optimization

Academic Year: 2017-18

Date: 22-09-2017

B.Tech III-I SEM

DAY WISE ATTENDANCE SHEET

SECTION: ECE-B

S.No	Roll Number	22-Sep-17	23-Sep-17	25-Sep-17	26-Sep-17	27-Sep-17
1	15UPIA0443	Mara	Mara	Mara	Mara	Mara
2	15UPIA0444	Keo	Keo	Keo	Keo	Keo
3	15UPIA0445	Priya	Priya	Priya	Priya	Priya
4	15UPIA0447	Bharathi	Bharathi	Bharathi	Bharathi	Bharathi
5	15UPIA0448	Ravali	Ravali	Ravali	Ravali	Ravali
6	15UPIA0449	Sua	Sua	Sua	Sua	Sua
7	15UPIA0450	Joshna	Joshna	Joshna	Joshna	Joshna
8	15UPIA0451	G. Nikitha	G. Nikitha	G. Nikitha	G. Nikitha	G. Nikitha
9	15UPIA0452	A	A	A	A	A
10	15UPIA0453	Mounika	Mounika	Mounika	Mounika	Mounika
11	15UPIA0454	K. Rul	K. Rul	K. Rul	K. Rul	K. Rul
12	15UPIA0455	Bavya	Bavya	Bavya	Bavya	Bavya
13	15UPIA0456	Savya	Savya	Savya	Savya	Savya
14	15UPIA0457	Se	Se	Se	Se	Se
15	15UPIA0459	Ramya	Ramya	Ramya	Ramya	Ramya
16	15UPIA0460	Sirija	Sirija	Sirija	Sirija	Sirija
17	15UPIA0461	S	S	S	S	S
18	15UPIA0462	Chandana	Chandana	Chandana	Chandana	Chandana
19	15UPIA0463	S	S	S	S	S
20	15UPIA0464	Shiva	Shiva	Shiva	Shiva	Shiva
21	15UPIA0465	Pravalika	Pravalika	Pravalika	Pravalika	Pravalika
22	15UPIA0466	Sravya	Sravya	Sravya	Sravya	Sravya
23	15UPIA0467	S	S	S	S	S
24	15UPIA0468	Arul	Arul	Arul	Arul	Arul
25	15UPIA0471	Kavya	Kavya	Kavya	Kavya	Kavya
26	15UPIA0472	Priya	Priya	Priya	Priya	Priya
27	15UPIA0473	Mang	Mang	Mang	Mang	Mang
28	15UPIA0474	Aranya	Aranya	Aranya	Aranya	Aranya
29	15UPIA0475	Prityanka	Prityanka	Prityanka	Prityanka	Prityanka
30	15UPIA0476	N	N	N	N	N
31	15UPIA0477	De	De	De	De	De
32	15UPIA0478	Mahathi	Mahathi	Mahathi	Mahathi	Mahathi
33	15UPIA0480	V. Rul	V. Rul	V. Rul	V. Rul	V. Rul
34	16UP5A0401	Divya	Divya	Divya	Divya	Divya
35	15C31A0432	R	R	R	R	R

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 29-09-2017

PROGRAM REPORT

Name of the Add on Course: Latest trends in chip design for Area and Power Optimization

Day/Duration: 35 Hours

Time: 4pm to 5pm

Resource Person: Mr. ARJUN MODI, Technical Manager in AMTRONICS, Hyderabad

Name of the Coordinator: G. Narendra, Assistant Professor Dept. of ECE VMTW, Hyderabad

Number of the Participants: 71

Topics covered: The following topics covered in this program

1. Analog IC Design
2. Digital IC Design


Course Outcomes:

COs	At the end of the course, students will have the ability to:	Pos Mapped	Strength of mapping
CO1	Develop mathematical models for modern MOS devices.	PO2,PO3	2
CO2	Develop solution to overcome short channel issues	PO3,PO4	3
CO3	Develop various compact models appropriate for industry.	PO3,PO4	2
CO4	Analyse current distribution in the devices like transistors, MOS devices.	PO2,PO4	2
CO5	Construct the circuit layout using the design rules	PO2,PO4	3

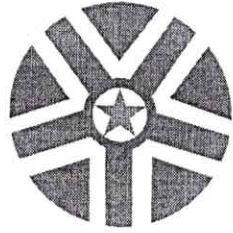
Assessment Procedure: The assessment of the Add on course is conducted in Multiple Choice Questions through offline Mode.


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Certificate of Course Completion

This is to certify that Ms./Mr. **GIUNDA DEVIKA**

Roll No. **15UPIA0416** Year **III**

has successfully completed the Add-On / Certification Course on

..... **Latest Trends in chip design for Area and Power Optimization**

held from **18-08-2017** to **27-09-2017**



HoD, ECE

Head of the Department

Electronics and Communication Engineering
Vignans Institute of Management and Technology for Women
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Telangana State

Principal, VMTW

PRINCIPAL

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