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1	Dr. S. Ranga Swamy et al	NA	An Enhanced Multi-Layer Neural Network to Detect Early Cardiac Arrests	IEEE Conference	5th International Conference on Electronics, Communication and Aerospace Technology, ICECA 2021 RVS Technical Campus, Coimbatore	International	2021	978-1-6654-3524-6	VMTW	IEEE	https://ieeexplore.ieee.org/document/9675882
2	Mr. G. Narendra et al	Global Emerging Innovation Summit (GEIS-2021)	Wearable Antennas-An Overview	NA	Global Emerging Innovation Summit	International	2021	978-1-68108-901-0	VMTW	Bentham Science	https://www.eurkaselect.com/197609/chapter/wearable-antennas-an-overview



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3	Dr. Samiran Chatterjee et al	Lecture Notes in Electrical Engineering	Printed Antenna for C-Band communication	Springer Conference	3rd International Conference on Communication, Devices and Computing	International	22021	978-981-16-9154-6	VMTW	Springer, Singapore	https://content.e-bookshelf.de/media/reading/L-17729161-d86c70c0db.pdf
4	Mr. P. Hari Krishna et al	NA	Classification of Cardiac Arrhythmias using Recurrent Neural Network and selected features	IEEE	5 th International Conference on Information System & Computer Networks	International	2021	978-1-6654-4787-4	VMTW	IEEE	https://ieeexplore.ieee.org/document/9702475




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5	Dr Raja Krishn Moorthy et al	NA	Multi-Parameter Smart Health Monitoring System Using Internet of Things	NA	International Online Conference on "Artificial Intelligence and Machine Learning Enabled 5G Networks: Recent Advances and Challenges (ICAMW-2021)	International	2021	NA	VMTW	NA	NA
6	Mr. M. Vishnu Vardhana Rao et al	NA	Data Mining Technique For Structural Strength Monitoring System Methodologies	IEEE	International Conference On Computer Communication And Informatics	International	2021	978-1-7281-5875-4	VMTW	IEEE Digital Library Xplore	https://ieeexplore.ieee.org/abstract/document/9402640
7	Mrs. K. Prathyusha et al	NA	COVID-19 in India: Lockdown analysis and future predictions using Regression models	IEEE	11th International Conference on Cloud Computing, Data Science & engineering -2021	International	2021	978-1-6654-1451-7	VMTW	IEEE	https://ieeexplore.ieee.org/document/9377052




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8	Mr. A. Mallikarjun et al	Advances in Sustainability Science and Technology	Investigation of Structural and Optical Properties of PMMA/PVdF-HFP Polymer Blend System	Proceedings of Fourth International Conference on Inventive Material Science Applications	Fourth International Conference on Inventive Material Science Applications	International	2021	978-981-16-4321-7	VMTW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-16-4321-7_26
9	Mr. Vijaykumar R. Urkude	Algorithms for Intelligent Systems	Design Optimization and Fault Tolerance in Network-On-Chips	Proceedings of Integrated Intelligence Enable Networks and Computing	Proceedings of Integrated Intelligence Enable Networks and Computing	International	2021	978-981-33-6306-9 978-981-33-6307-6	VMTW	Springer, Cham	https://link.springer.com/chapter/10.1007/978-981-33-6307-6_51#citeas
10	Mr. E. Nagaraj et al-2021	NA	Design and analysis of low power Hybrid Full adder using CMOS 45nm Technology	NA	3rd International Conference on Communication, Devices and Computing	International	2021	NA	VMTW	NA	NA




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10	Mr. Vijaykumar R. Urkude	Block chain Technology: Applications and Challenges	Anatomy of Block chain Implementation in Healthcare	NA	NA	NA	2021	978-3-030-69394-7 978-3-030-69395-4	VMTW	Springer, Cham	https://link.springer.com/chapter/10.1007/978-3-030-69395-4
11	Dr. C. Srinivasa Kumar et al	NA	Software defect prediction using optimized cuckoo search based nature inspired technique	Smart Computing Techniques and Applications	Fourth International Conference on Smart Computing and Informatics	International	2021	978-981-16-1502-3	VMTW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-16-1502-3_19




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12	Dr. S. Ranga Swamy et al	Proceedings of First International Conference on Mathematical Modeling and Computational Science	Auto-adaptive Learning for Machine Perception of Native accent using Deep Learning	Advances in Intelligent Systems and Computing	First International Conference on Mathematical Modeling and Computational Science	International	2021	978-981-33-4389-4	VM/TW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-33-4389-4_58
13	Dr. S. Ranga Swamy et al	Lecture Notes in Networks and Systems	An Energy-efficient PSO based Cloud Scheduling Strategy	Innovations in Computer Science and Engineering	Springer Proceedings-Lecture Notes in Networks and Systems	International	2021	978-981-33-4543-0	VM/TW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-33-4543-0_79




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14	Mr. J. Sunil Kumar et al	Algorithms of Intelligent Systems	Assessment On the Adequacy of Dual Current Supply in CMOS Dual Differential Amplifier	NA	1 st International Virtual Conference on Integrated Intelligence Enable Networks and Computing	International	2021	978-981-33-6306-9 978-981-33-6307-6	VMTW	Springer, Singapore	https://Link.Springer.Com/Chapter/10.1007/978-981-33-6307-6_5
15	Dr. S. Ranga Swamy et al-2021	Introduction to Machine Learning- A Perspective Approach	NA	NA	NA	NA	2021	978-93-90761-21-0	VMTW	Shashwat Publication	https://www.amazon.in/Introduction-Machine-Learning-Perspective-Approach-ebook/dp/B093T2LQJ2



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16	Dr. Samiran Chatterjee et al	NA	Low Power High Speed Design Of 4 Bit Ripple Carry Adder Using Domino Logic	Turkish Online Journal of Qualitative Inquiry	sustainable Innovation in Science & Technology	International	2021	NA	VMTW	Scopus	https://www.tojqi.net/index.php/journal/article/view/3385/2294
17	Mrs. M. Hemalatha et al-2021	NA	Low Power High Speed GDI 4 Bit RCA Circuit Design Using 45nm CMOS Technology	Turkish Online Journal of Qualitative Inquiry	International Conference on sustainable Innovation in Science & Technology	International	2021	NA	VMTW	Scopus	https://www.tojqi.net/index.php/journal/article/view/3386/2295




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18	Mr. J. Sunil Kumar et al	Algorithm's of intelligent systems	Design and implementation of High Speed and large bandwidth voltage follower using CMOS technology	NA	1 st International Virtual Conference on Integrated Intelligence Enable Networks and Computing	International	2021	978-981-33-6306-9 978-981-33-6307-6	VMTW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-33-6307-6_88
19	Mr. J. Sunil Kumar et al	NA	High Performance Digital to Analog Converter Using CMOS 45nm Technology	NA	6th International Conference on Inventive Computation Technologies	International	2021	978-1-7281-8501-9	VMTW	IEEE	10.1109/ICICT50816.2021.9358566




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20	Dr. S. Ranga Swamy et al	Algorithms for Intelligent Systems	An aviation delay prediction and recommendation system using Machine Learning Techniques	Proceedings of Integrated Intelligence Enable Networks and Computing	1 st International Virtual Conference on Integrated Intelligence Enable Networks & Computing (IIENC-2020)	International	2021	978-981-33-6307-6	VMTW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-33-6307-6_25
21	M. Vishnu vardhana rao et al	Algorithms for Intelligent Systems	Structural Strength Monitoring System Practices using Machine Learning	Proceedings of Integrated Intelligence Enable Networks and Computing	1 st International Virtual Conference on Integrated Intelligence Enable Networks & Computing (IIENC-2020)	International	2021	978-981-33-6307-6	VMTW	Springer, Singapore	https://link.springer.com/chapter/10.1007/978-981-33-6307-6_26




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An Enhanced Multi Layer Neural Network To Detect Early Cardiac Arrests

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Abstract- Patients and doctors are paying increasing attention to health-care automation because it can save a person's life by predicting ailments early. Many people are suffering from chronological diseases as a result of altering eating habits, regardless of age or gender. "Heart Attacks" is a severe ailment that requires attention from time to time. To date, all automated systems have built models using either classical or ensemble machine learning techniques. Overfitting has affected only a few of these systems, such as random forest and SVM algorithms. As a result, the proposed approach has chosen the "Multi Layer Preceptron" neural network technique, which solves the problem of overfitting and generates an accurate number of correct labels linked with the training model. Instead of using all of the variables mentioned in the dataset, the suggested method assists clinicians in predicting a heart attack in a user at an early stage by assessing only 7 top informative attributes. The model was also compared to other classifiers in order to establish the state of the art, which was determined to be "97.23 percent."

Keywords: Feature Engineering, Greedy Genetic Algorithm, 8- Layered Multi Layer Preceptron Architecture, Ensemble Algorithm, Meta Classifier

I. INTRODUCTION:

Classification is type of supervised machine learning algorithm, which defines a mapping function to draw a relationship between set of inputs and class labels defined in the dataset. The types of machine learning algorithms are shown in figure 1.

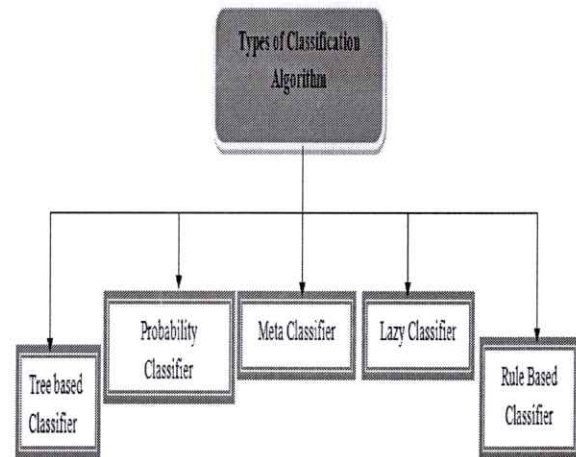


Figure 1: Categories of Classification Algorithm

In Tree based classifier, the proposed system has chosen J48 Algorithm to identify whether a person suffer from heart attack or not by constructing tree based on entropy as decision parameter. Among all the trees, J48 is considered as best decision tree algorithm because it evaluates all the possible subsets and generates the tree as shown in figure 2.

Conditional independence is important in determining the impact of attributes on the class label parameters in a probability classifier. The Bayesian probability, which is popular for generating precise values based on decision rules, is used in conditional probability. The suggested system used a naive Bayesian approach, which yielded positive outcomes during the prediction phase. The



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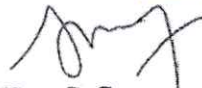
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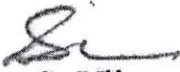
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CHAPTER 32

Wearable Antennas-An Overview

Narendra Gali^{1*} and Narbada Prasad Gupta²¹ Lovely Professional University, Punjab/Assistant Professor, Vignan's Inst. of Mgmt. and Tech. for Women, Hyd., India² School of Electronics and Electrical Engineering Lovely Professional University, Punjab, India

Abstract: The most popular antenna for portable devices in current communication technologies is the wearable antenna due to its compactness and flexibility; demand was rapidly growing and can communicate through signals with the human body and the wearable devices. The advantages of wearable antennas are flexible, hidden, low profile, and no harm to humans. The key benefit of this antenna is that it is placed on the human body or included in clothing, effortlessly transmits, and receives signals through clothes or on-body. These antennas play a vital role in the number of applications, viz. navigation (118MHz to 137MHz), medicine (750MHz to 2.6GHz), military (225MHz to 400MHz), RFID (433MHz to 5.4GHz), physical training, tracking, and health monitoring, etc. This paper discussed the important aspects of wearable antennas, which include materials used, substrate, and fabrication techniques. Next, discussed a clear overview of wearable antennas existing and design aspects, their advantages, and drawbacks.

Keywords: Fabrication Technique, Flexible Antennas, ISM Band, Substrate Integrated Waveguide, Textile Antennas, Wearable Antennas.

1. INTRODUCTION

It has been seen that during the last decade of years, portable devices play a proximity role in human life those are mobiles and tablets. The technology is rapidly changing year by year and the size of the device, visibility decreases. In forthcoming days, sensors are used to control human activities; further devices are used to monitor the different requirements of the human including medical

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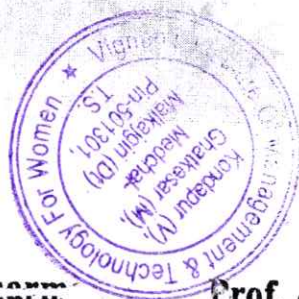
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Abstract



Document Sections

- I. Introduction
- II. Related Work
- III. Proposed Methodology
- IV. Experimental Results
- V. Conclusion

Abstract:The most frequent kind of heart ailment is cardiac arrhythmia (also known as a tachycardia). The computer-based decision-making method is quite beneficial in the analysis... **View more**

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Abstract:

The most frequent kind of heart ailment is cardiac arrhythmia (also known as a tachycardia). The computer-based decision-making method is quite beneficial in the analysis of the Electrocardiogram (ECG) signal and the categorization of CAs, among other things. This research describes an automated categorization of CA's that combines chosen aspects of the ECG signal with a Bidirectional Long Short-Term Memory (BLSTM) network, which is described in detail elsewhere. The linear and non-linear components of the ECG data were extracted and input to two BLSTM networks, which were then coupled together in a fully connected layer. BLSTM networks are the most extensively used recurrent neural networks for evaluating sequential data and are also the most widely used recurrent neural networks. All of the characteristics of the segmented heartbeats are retrieved. The five main forms of CAs are discussed in detail. Normal beat (N), Left Bundle Branch Block (L), Right Bundle Branch Block (R), Premature Ventricular Contraction (V), and paced beat (P) are the five kinds of heartbeats (Q). The findings demonstrate that the BLSTM model, which incorporates both linear and nonlinear characteristics, achieves the maximum accuracy in the classification task at hand.

Published in: 2021 5th International Conference on Information Systems and Computer Networks (ISCON)

Date of Conference: 22-23 October 2021 INSPEC Accession Number: 21664954

Date Added to IEEE Xplore: 14 February 2022

DOI: 10.1109/ISCON52037.2021.9702475

Publisher: IEEE

ISBN Information:

Conference Location: Mathura, India

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ELSEVIER
Computers & Electrical Engineering
ISSN: 0045-7906

ICAMW - 2021

IJARSCIT
Impact Factor: 4.819
www.ijarscit.com
ISSN- 978-93-91265-21-2



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DATA MINING TECHNIQUE FOR STRUCTURAL STRENGTH MONITORING SYSTEM METHODOLOGIES

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Abstract— Natural Hazards are the current issues to effect the Building infra-Structures. But the difficult task is to know the status of Building infra-structures, in terms of life time, strength, quality and status of damages in the structures of the buildings. As on today, any automatic methodology are not available for predict or estimate the damages in the infra-structures of the buildings. So essential maintenance can be required. Structural Strength Monitoring System (SSMS) are one of the automatic Monitoring System for satisfying the requirements like predicating damages, classification of damage structures. When SVM classifier is used for calculating the strength of the structures, it cannot effectively handle large data received from big structures but its accuracy for handling small structures is good and ANN classifier handles large amount of data gathered from sensors but its accuracy is low. To design a framework which can effectively handle large amount of data and to improve accuracy rate a hybrid algorithm combining the features of Rough set Support vector machine (RS-SVM) classified structures and Rough set Artificial Neural Network (RS-ANN) is proposed. Structural Strength Monitoring System (SSMS) utilizing Wireless Sensor Systems (WSS) has picked up research interest because of its capacity to reduce the expenses related with the establishment and upkeep of SSMS frameworks. This methodology contains, the combination of both feature subset reduction methods like Rough set theory (RST), Mutual Information (MI) etc. and Classification methods in Data-Mining like SVM, ANN etc.

Keywords-component; Artificial Neural Network (ANN), Mutual Information (MI), Rough set theory (RST), Structural Strength Monitoring System (SSMS), Support Vector Machine (SVM), Wireless Sensor Systems (WSS)

1. INTRODUCTION

CRED (Center for Research on the Epidemiology of Disasters) are the one of the best estimated organization for annual statistical review of the Natural Disasters [1]. Result of this organization show that the total number of disasters are 392 in the year of 2019. This number is less than the average from 2010 to 2018 (376.4). The costs of damage from natural disasters were reported to be 12% higher (US \$154 billion) than the 2010–2018 average. 47% of the world's 395 disasters occurred in Asia.

One place for living the humans are called Building. Building having the different characteristics like age, floor area and presence of plan irregularity are used as basic features or variables for the predicating the damage features or predictor variables for the machine learning models. One of the reason for increasing the occurrences of Natural Disaster is climate changes. From 1950s, the rate of increasing the changes in the climate are goes very high. The deviations in climate are proposed to upsurge the risks to humans. The damage caused by natural disasters to buildings is affected by various factors such as weather conditions, the environment in which the buildings are located, and structure of the buildings [2]. Easterling et al argued that if there are identifiable trends in extreme climatic events such as temperature or precipitation, human impacts on climate change are a very important factor in damage caused to buildings from natural disasters. G.P.Cimellaro et al. make an effort on physical infrastructure interdependency for statistical analysis about the causes and consequences of building damage triggered by natural disasters [3]. Chandler et al. [6] develop the estimate method for damage assessment and fixed the parameters or features of the building structures, for example occupancy, age, interior, exterior and height. In this estimate method, vulnerability curves are used for assess the damages in the building infrastructures. B. Konukcu et al. [7] says that no.of floors, type of construction are also used as the impact parameters for evaluate the effect of disasters on buildings by updating the building damage dataset of Istanbul. Blong et al. [5], the assessment of damage to residential buildings is the most important because they represent more than half of all constructed space. Irrespective of disaster type, the strength of the damages in the buildings are increases every year. Therefore, the disasters are directly or indirectly show the impact on the number of people and associated with the costs [4]. So the major task is to prevent or mitigate the damages. Physical verification of building infrastructures are the first method for mitigate the damages. Manual workers are needed for both classification of structures and physical verification for the identifying the damages in the buildings and its structures. So automation and numerical analysis are used for analysis of building damage triggered by natural disasters which helps to mitigate or reduce the damage, cost.



Jun 2019

COVID-19 in India: Lockdown analysis and future predictions using Regression models

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Abstract – The new virus named COVID-19 identified in Wuhan, China causes a severe impact on the respiratory system of the human. In considering its effect and spread in the community, the Government of India has imposed World's biggest Lockdown from 25th March 2020. Later on, it was extended in another three phases as Lockdown 2.0, 3.0, and 4.0 with some relaxations in each Lockdown. In this paper, we have studied the COVID-19 patients' data of Confirmed cases, Recovered cases, and Deaths based on before, after, and during lockdowns. The data analysis is done basing on the daily growth rate of confirmed cases, recovery rate, and fatality rate. We have applied Regression techniques viz., Linear Regression, Polynomial Regression of Machine Learning (ML) to predict the future spread of this virus in India. The Polynomial Regression has given accurate predictions comparing with the Linear Regression.

Keywords – Lockdown, COVID-19, Linear Regression, Accuracy metrics, Polynomial Regression.

I. INTRODUCTION

The world is facing one of its most horrible crises regarding public health due to COVID-19, which was first identified in China in late December 2019 [1]. Infection of this virus is no longer limited to Wuhan. By January 2020 nine cases of COVID-19 infection have been stated in Thailand, Japan, Korea, USA, Vietnam, and Singapore through air travel is likely [2][3]. It has spread to almost all parts of the globe with major impacts on health and the economy. The World Health Organization (WHO) has warned that the COVID-19 pandemic is deteriorating worldwide and things won't return to the old normal for some time [4] [5] [6] [7]. An important source for infecting this virus is asymptomatic carriers. Fever, cough, and breathing problems are important symptoms and the infection can be transmitted during the incubation period [8]. The infection rate of COVID-19 looks to be greater than that for the seasonal flu and MERS, with the kind of possible estimates covering the infection rates of SARS and Ebola.

In India, the first COVID-19 case is confirmed on 30th January 2020 in Kerala state. By March 4th, the country has witnessed a sudden jump of 29 cases. The positive cases crossed 100 by March 15th, 2020. The Government has called for a "Janata Curfew" on 22nd March. To face this pandemic, the Government of India has imposed Lockdown for three weeks from 25th March 2020 to 1st April 2020. By the end of March, the number of cases crossed 1000. The Lockdown is further extended in three phases as 2.0, 3.0,

and 4.0 with phase by phase relaxations. On 30 May, the Government stated that the current lockdown would be more prolonged till 30 June in containment zones, with amenities restarting in a phased manner, beginning from 8 June, in other zones. It is termed as "Unlock 1.0" and is stated to "have an economic focus".

Machine Learning (ML) is to acquire more valuable statistics from a large amount of data using an algorithm model for explicit problems. Applications of ML extend to computer science, medicine, statistics, psychology, engineering, etc. ML can be used to handle large data and intelligently predict the spread of the disease. ML can be accomplished in a Supervised or Unsupervised way. In Supervised learning, the system gets a dataset with different example parameter values and decisions/ classification, from which it assumes a mathematical function, which automatically maps input features to a target feature. On the other hand, Unsupervised learning means that the system acts and notices the consequences of its actions, without referring to any predefined type cases other than those observed earlier. In this paper we implemented two Regression models which fall under Supervised learning – Linear Regression, Polynomial Regression on the COVID-19 dataset for future prediction of Confirmed, Recovered, and Death cases in India.

The rest of the paper is organized into four sections. Section 2 presents the Exploratory Data Analysis (EDA) and Lockdown wise analysis is discussed in Section 3. Section 4 we have implemented ML models for future predictions on the COVID-19 dataset. The paper is concluded in the Section 5.

II. EXPLORATORY DATA ANALYSIS (EDA)

Exploratory Data Analysis (EDA) is the first and important step to analyze data and to summarize the characteristics using visualization techniques. This makes us identify the best features required for the Machine Learning (ML) model. The EDA will use tools like correlation matrix, heat map, plots, and frequency distribution to understand and explore the data set.

A. Understand Dataset

The datasets used in this are downloaded from the Kaggle repositories. The dataset complete.csv consists of date wise and state wise data along with the following features.

Date	Date of recording data
Name of State / UT	State or Union Territory name





Proceedings of Fourth International Conference on Inventive Material Science Applications pp 295–306

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Investigation of Structural and Optical Properties of PMMA/PVdF-HFP Polymer Blend System

[Maheshwar Reddy Mettu](#), [A. Mallikarjun](#), [M. Vikranth Reddy](#), [M. Jaipal Reddy](#) & [J. Siva Kumar](#)

Conference paper | [First Online: 20 October 2021](#)

548 Accesses | **2** Citations

Part of the [Advances in Sustainability Science and Technology](#) book series (ASST)

Abstract

The polymer PMMA and PVdF-HFP blend polymer films have been prepared by solution casting technique. These blending polymer films were investigated by X-ray diffraction (XRD), scanning electron microscopy (SEM), FTIR and UV optical absorption techniques. The peaks of PMMA are disappeared gradually with blending of PVdF-HFP which is revealed by XRD where structure modified semi-crystalline to amorphous phase. PMMA surface morphology reveals a rough surface. SEM



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Design Optimization and Fault Tolerance in Network-On-Chips



Vijaykumar R. Urkude

Abstract Network-on-chip (NoC) is a rising worldview for on-chip data transfer of vast VLSI systems actualized on one chip. System architecture of NoC mounts processor centers, memory centers, and specialized intellectual property (IP) squares trade data on an on-chip network. NoC replaces committed, design-explicit interconnection (transports, point-to-point ports, and so on.) in system-on-chip (SoC) with adaptable, universally useful network. SoC sets up a correspondence between the modules under the imperative of deadlock opportunity. We make utilization of the intrinsic repetition in NoCs because of numerous ways between parcel sources and sinks and propose distinctive fault-tolerant routing schemes to accomplish much preferred fault tolerance abilities over conceivable with traditional routing schemes. This paper focused on the concept of NoC, its design space and automation tools, NoC architecture, optimization of network, algorithms, and fault tolerance in NoC.

Keywords Fault · Network-on-chip · Routing · System-on-chip

1 Introduction

Developing interest of capacity in the electronics devices, we have to suit numerous highlights in the chip. What is more, this has conceived an offspring of another measurement called system-on-chip (SoC). SoC is to get organized like interconnections which is called network-on-chip (NoC) design [1]. The switch-based interconnection instrument gives a lot of versatility and adaptability from the obstruction of complex wiring. Substitution of SoC transports by NoCs offers high versatility and the ordinariness of a system structure. The NoC similarly reduced the SoC fabricating cost, SoC time to advertise, SoC time to volume, and SoC setup possibility. The NoC approach has an obvious ideal position over ordinary transports and most exceptionally structure throughput. The requests of crossbars or multilayered transports have characteristics some place amidst customary transports.

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K. K. Singh Mer et al. (eds.) *Proceedings of Integrated Intelligence Enable Networks and Computing, Algorithms for Intelligent Systems*,
https://doi.org/10.1007/978-981-330-630-7_6 51



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Blockchain Technology: Applications and Challenges pp 51–76

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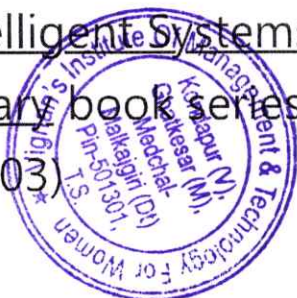
Anatomy of Blockchain Implementation in Healthcare

[Shubhangi V. Urkude](#) , [Himanshu Sharma](#), [Seethamsetty Uday Kumar](#) & [Vijaykumar R. Urkude](#)

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Software Defect Prediction Using Optimized Cuckoo Search Based Nature-Inspired Technique



C. Srinivasa Kumar, Ranga Swamy Sirisati, and Srinivasulu Thonukunuri

Abstract These days, software systems are very complex and versatile. Therefore it is essential to identify and fix the software error. Software error assessment is one of the most active areas of research in software engineering. In this research, we are introducing soft computing methods to assess software errors. Our proposed technique ts software gives errors and accurate results. In our proposed method, the error database is first extracted, which acts as an input. After that, the collected input (data) is clustered by the clustering technique. For this purpose, we use the modified C-Mean Algorithm. Therefore, the data is clustered. An efficient classification algorithm then groups clustered data. For this reason, we use a hybrid nervous system. Therefore, there are software bugs, and these errors are optimized using the MCS algorithm. Our proposed method for software error assessment is implemented on the Java platform. Performance measurement is measured by various parameters such as execution rate and execution time. Our proposed Cuckoo search based strategy is comparable to many existing strategies. Graphical representation of comparison results from our proposed strategy for identifying software proposals is one that effectively evaluates profitable strategy and reasonable reference rates.

1 Introduction

Software Defect Prediction (SDP) plays an essential part in reducing software development costs and maintaining Achilles' and others' high quality (2017). When there is a recurring software failure in the system, it automatically causes a software error. Software error is a bug introduced by software developers and shareholders. A software vulnerability assessment's primary purpose is to improve the quality,

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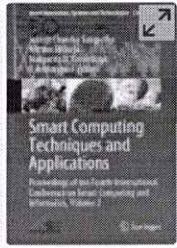
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S. Sathya et al. (eds.), *Smart Computing Techniques and Applications*,
Smart Innovation, Systems and Technologies 224, PRINCIPAL
https://doi.org/10.1007/978-981-16-1502-3_19

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Smart Computing Techniques and Applications pp 183–192

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Software Defect Prediction Using Optimized Cuckoo Search Based Nature-Inspired Technique

[C. Srinivasa Kumar](#), [Ranga Swamy Sirisati](#) & [Srinivasulu Thonukunuri](#)

Conference paper | [First Online: 14 July 2021](#)

416 Accesses | **1** Citations

Part of the [Smart Innovation, Systems and Technologies](#) book series (SIST, volume 224)

Abstract

These days, software systems are very complex and versatile. Therefore it is essential to identify and fix the software error. Software error assessment is one of the most active areas of research in software engineering. In this research, we are introducing soft computing methods to assess software errors. Our proposed technique ts software gives errors and accurate results. In our proposed method, the error database is first extracted, which acts as an input. After that, the collected input (data) is


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Auto-Adaptive Learning for Machine Perception of Native Accent Using Deep Learning



Mekala Srinivasa Rao, P. S. V. Srinivasa Rao, and S. Ranga Swamy

Abstract One of the solutions to artificial intelligence is machine learning. It enables us to create machines that can learn from experience rather than be programmed explicitly. Current formulations of machine learning are mostly designed with the help of data available for learning and performing specific tasks from neural networks. Deep learning is an effective machine learning approach that can solve multiple and specific tasks with mini mother change. Deep learning extends machine learning to multi-level distributed representations with the necessary mapping functions into a single composite function, and in particular neural networks. Along with their capability to learn dynamic hierarchical representations, the advent of deep learning and neural networks has opened up the way for continuous training. The main objective of this thesis is to research and establish a systematic approach to continuous learning that facilitates the success of profound education and neural networks.

Keywords Deep learning · Machine learning · Artificial intelligence · Neural networks

1 Introduction

Based on current artificial intelligence (AI) research, the imitation of a typical human brain. Computers are faster than humans but not smarter than human brain, because the human brain has much intelligence than a computer. That is.

- Recognizing
- Accepting
- Listing
- Feeling
- Intellectual

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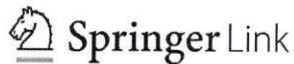
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S.-L. Peng et al. (eds.), *Proceedings of First International Conference on Mathematical Modeling and Computational Science*, Advances in Intelligent Systems and Computing 1292, https://doi.org/10.1007/978-981-33-4389-4_58

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An Energy-Efficient PSO-Based Cloud Scheduling Strategy

Innovations in Computer Science and Engineering pp 749-760 | Cite as

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Conference paper

First Online: 24 April 2021

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Part of the [Lecture Notes in Networks and Systems](#) book series (LNNS, volume 171)

Abstract

Cloud computing provides useful services to users with extensive and scalable resources that virtualized over the internet. It defined as a collection of the communication and computing resources located in the data-center. The service based on on-demand is subject to QoS, the load balance, and certain other constraints with a direct effect on the user's consumption of resources that are controlled by this cloud infrastructure. It is considered a popular method as it has several advantages that have been provided by a cloud infrastructure. The cloud scheduling algorithm's primary goal was to bring down the time taken for completion (the cost of execution) of the task graph. The start time and the finish time for the task node influence the task graph completion completed to the time (the cost). The task node sort order an essential aspect that influences the start time and the finish time for every task node. In a hybrid cloud, efficient dense particle mass-based cloud scheduling is efficient because users need to maintain the security of the hybrid cloud. Different algorithms with different algorithms suggested by researchers in the cloud. This paper proposes particle swarm optimization (PSO)-based cloud optimal scheduling. Effective results obtained in an efficient fuzzy mass-based PSO cloud scheduling.

Keywords

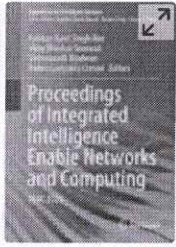
Cloud scheduling Particle swarm optimization Cloud tasks Load balance

Fuzzy sets

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Proceedings of Integrated Intelligence Enable Networks and Computing
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Assessment on the Adequacy of Dual Current Supply in CMOS Dual Differential Amplifier

[Venkateswarlu Mukku](#)  & [J. Sunilkumar](#)

Conference paper | [First Online: 24 April 2021](#)

602 Accesses | **1** [Citations](#)

Part of the [Algorithms for Intelligent Systems](#) book series (AIS)

Abstract

This paper proposed a method, which aims to increase the fault detection and mitigate faults which are identified in CMOS analog and digital circuits. This proposed technique is applied to a typical dual differential CMOS circuits. The proposed test includes a dual current-based test technique, which needs a fault-free circuit which combines with quiescent supply current and transient supply current methods to provide a fault confirmation by providing some known faults. A built-in dual current supply technique, which



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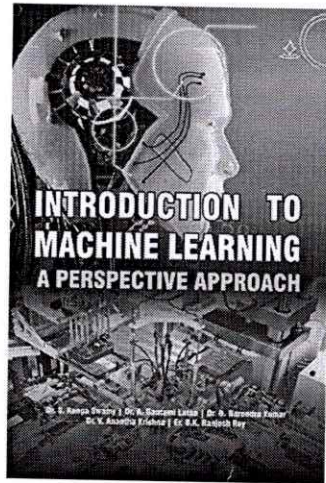


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Machine learning was built from an engineering perspective, while machine learning was born out of a computer science approach. In the one side the operations may be looked at as two different areas, but they have grown in tandem over the past years and around the same period. Other than the univariate methodology (the conventional way of doing things), there has been a great rise in non-uniform approaches. , algorithmic and graphical simulations are being used for statistical and quantitative trading in all kinds of markets. Also, the functional applicability of Bayesian approaches has been significantly improved by the development of a variety of

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- Publisher : Shashwat Publicaton (28 April 2021)
- Language : English
- File size : 4364 KB
- Text-to-Speech : Not enabled
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Low power High Speed Design of 4BIT Ripple Carry adder using Domino logic

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Abstract

Accurate domino logic circuit keeper control can enlarge the performance, speed. Although, keeper feedback circuit is correlated with the positive feedback gain excessively delay variability is expanded. The main aim is to decrease the delay and reduce the loop gain effect, here domino clock delayed dual keeper (CDDK) circuit is conferred .During the commencing estimation phase, disabled the two keeper devices of the keeper circuit in CDDK domino structure. By decreasing the dispute current concurrently the circuit speed of operation is intensified. The carried out various metrics and outcomes are analyzed for the circuit simulations .Moreover , the simulations are accomplished on a 4-bit ripple adder using structure of CDDK demonstrate decreased characteristics of delay variability due to the domino CDDK structure smaller loop gain in opposition of domino circuit The demonstration of intensified by turn down variance current. Through the counterpart of domino logic circuits in opposition of comparison outcomes are validated. By using this tanner power consumption is around 8 micro watts. The analyzing of circuits is carried out using standard CMOS tanner tool using library of 45nm technology.

Keywords— Domino logic, delay, domino ripple adder low power consumption.

I. INTRODUCTION

Very large scale integration technology [1] is a methodology in which more number of transistors are fabricated on silicon area. In CMOS technology dynamic logic method play an important role in designating more logic circuits. By using dynamic logic method we can optimize more number of parameters related to digital engineering. Dynamic logic methodology plays an important role in VLSI. This will increase the operation of the circuits. To implement dynamic logic circuit on silicon it consumes less space when compare to the static transistor technology. By using this dynamic logic circuits to design any digital circuit it becomes more complicated rather than static transistors. And also to perform it will consume more power. Power consumption by the dynamic logic circuit is more and power delivered to the load is less, if power delivered [2] to the load is less which will decreases the circuit's efficiency. So to enhance the performance of the dynamic logic circuit, and to decrease the delay, to reduce the power consumption. To avoid all stated problems domino logic circuit arrangement is well suited. Due to low noise margin the speed of the domino logic circuit is more compared to static logic gates. In large circuit implementation domino logic circuit operation will play an important role. Which will consumes less space and increased the operation of the circuit compared to the static conventional CMOS circuit. Domino logic circuit arrangement is well suited at integration of more number of circuits on silicon.

Domino addressing a extreme impact in the essential applications of consumption of low power and high-speed [3], like as comparators tag, read out register the paths, programmable encrypt, memories of multiport and SRAM pre-decrypt gate, by the utilization of domino logic style the fan-in gates wide realization is astounding



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Low Power High Speed GDI 4-bit RCA Circuit design using 45nm CMOS Technology

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Abstract

In Digital Engineering, if we want to design a 4Bit adder which is very essential component in an arithmetic logic circuit (ALU) and also plays a crucial role in all the computational circuits as well. In this paper, 4 bit ripple adder using a one bit full adder is designed at 45nm CMOS technology. to design a full adder, we require XOR, OR, AND logic gates, where we combine all the above logic gates to get a one bit full adder finally. The GDI (gate diffusion input) it is a technique in which number of transistors required to design specific application will gradually reduce. When it is compared with the conventional circuit, by using GDI not only reduces transistors count but also power consumption. The maximum power saving is of 93.04%, the delay is saved by 76.76% and coming to the overall PDP the saving is of 96.01%. By considering 4- full adders we can build a 4-bit ripple carry adder. Hence the whole designing can be done at supply voltage 1.8V as we are using 45nm CMOS technology.

Keywords— GDI Technique, OR gate, AND gate, 1 FA, 4 bit RCA, low Power consumption.

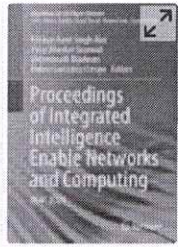
I. INTRODUCTION

Day by day electronic portable systems based on the battery usage demand is increasing, for driving the devices which are portable they require battery. In designing personally communicating devices, mobile phones, laptops and notebooks important concern is speed and power consumption. In VLSI technology [1-4] the parameter which plays important role is power consumption. For making circuitry cool we require cooling fan because of reducing battery life and increase in heating due to more power consumption. The cost of the whole system is affected and the battery life because of the more power consumption. Which discussed in the above devices and digital communication devices mostly are used in the applications such as microcontrollers, video and image processing and digital signal processing operated in the different operations multiplication, addition, subtraction. In the adder cells internally the different operations are performed like multiplication, subtraction, addition. In the digital communication devices designing more vital role is played by the one bit adder. Addition operation is performed by integrating the 1-bit full adder cells [5] in multiple of number digital communication devices frequently, the whole system performance is determined by the adder cells and adder cells is the reason which plays an vital role.

The adder circuit performance and dissipation of power is affected due to the increase in the complexity of the circuit and chip area is reduced. To reduce the power dissipation and size of chip in VLSI design the circuit is concerned in low power. In MOSFET technology the number of types of dissipation of power is two types they are dynamic power dissipation and static power dissipation. The parameters which Effects the device of the static power dissipation are reverse - biased junction leakage, sub threshold leakage, gate induced drain leakage and gate direct tunneling leakage of scaling parameters effected majorly. Power of short circuit and switching are mainly considered in dynamic power dissipation. The theoretical calculations of dynamic power dissipation and static power dissipation respectively P_s is the product of the leakage current and supply voltage [6]. P_D is the product of half of the operating frequency, load capacitance with square of logic voltage swing. The different





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Proceedings of Integrated Intelligence Enable Networks and Computing
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Design and Implementation of High Speed and Large Bandwidth Voltage Follower Using CMOS Technology

[M. Srilakshmi Ravali](#) , [Lalitha Malladi](#) & [J. Sunilkumar](#)

Conference paper | [First Online: 24 April 2021](#)

616 Accesses

Part of the [Algorithms for Intelligent Systems](#) book series (AIS)

Abstract

Signal parameters are playing an important role in designing analog and mixed signal circuits. In this paper, we proposed a technic called modified conventional voltage follower. It is a technic which is used to enhance the bandwidth and slew rate. The proposed method has 60 MHz bandwidth, 22.5 V/ μ s slew rate, and FOM figure of merit of 52 (MHz \times pF/ μ W) for load capacitance = 20 pf. By this proposed method, higher current and higher bandwidth than the standard voltage follower by




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High Performance Digital to Analog Converter Using CMOS 45nm Technology

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Abstract - This article represents about 8-bit digital to analog converter (DAC). A digital to analog converter (DAC) takes a digital signal and converts it to an analog signal (i.e; continuous form) to drive the interfaces with the real-world such as a speaker in the cell phone or the LED display on your watch. As such, anytime a digital circuit has to interface to a display or a speaker or an antenna or any number of other devices that need to be driven by an analog input and required a digital to analog converter (DAC). Digital to analog converter (DAC) is more efficient and substantially more accurate to do signal processing in the digital domain (i.e language used by computers). This article represents a digital to analog converter (DAC). The DAC was implemented by using 45nm CMOS technology. It also consumes 1.46mW of power from 1.8v supply voltage. The noise margin of the DAC is 9dB.

Keywords—Current mirror, Differential amplifier, Common source amplifier, R-2R DAC

I. Introduction

The real-world information (or) data is in the form of analog. The storing of digital information (or) data is easy when compared to storing analog data. There are few benefits of storing digital information i) Analog information [1] requires more memory to store the digital form. ii) Digital signal contains less noise iii) Digital data is encoded and refuge features. In real-time applications digital to analog converter is used to receive the signal and analog to digital converter to send the signal through the transmitter. The analog data if interfaces the digital data [2] by using the [5] in real-world applications. The sensors to sense the environment changes and gives the output then transducer is used to convert any form of signal to the electrical signal and vice versa. There are many uses of DAC in electronic devices like in the i-phone because it is not having inbuilt headphones for converting audio, communications for converting digital data into analog data, mobile phones, etc. There are two types of DAC [3-6] they are summing amplifier and the R-2R ladder DAC. The output voltage of the DAC is 2.7v.

II. Literature survey

In [1], the author proposed a 65 nm CMOS 6-bit 60 GS/s Time Interleaved DAC with Full-Binary Sub-DACs. The more integrated DACs are interfacing with the multiple 2-channel 6-bit indistinguishable 20 Gs/s DACs. The DAC which has exactly two children or zero for each node makes the DAC firm and powerless. By the heterogeneous analog signal and enhancing timing remove the bug in the software in the major areas. The archetype DAC achieved a low figure of merit and a high SFDR ratio. In [2], the author proposed a 12-bit 20-MS/s SAR ADC with Fast-Binary-Window DAC Switching in 180nm CMOS. The main drawback of the DAC in is the total capacitance. This leads to the standardization of the capacitor technique which is typically used for a mismatch. The main usage of this standardization technique is to correct the errors in the capacitor by using digital post-processing by consuming additional power and implementing complicated hardware. Another scheme called capacitance swapping is introduced to improve the linearity of DAC by interchanging the total capacitance one half with the other half. To have finer linearity, DAC error which is caused by the capacitor mismatch through the MSB capacitor switching error is randomized it is removed to decrease the SNR [7] i.e signal to noise ratio. [2]. In [3], the author suggested a Systematic method to find an Optimized Quad-Quadrant Random Walk Sequence for reducing the Mismatch effect in Current Steering DAC. Linear distribution: The density of the oxide and stupefy of the wafer are the main causes for which linear error profile was shown in source current array $L(x, y) = gL * \cos \theta * x + gL * \sin \theta * y$ (Gradient angle is denoted by θ , gL is denoted by linear gradient slope). Quadratic distribution: Quadratic profile variation is shown by the mechanical stress on the temperature gradient and the die $Q(x, y) = gQ * x^2(x^2 - y^2) - a_0$ (parameters gQ and a_0 are the dependent on the technology). Joint distribution: It is the emplacement of linear



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An Aviation Delay Prediction and Recommendation System Using Machine Learning Techniques



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and Anga Gautami Latha

Abstract Aviation recommendation and delay prediction (ARDP) systems are data filtering strategies that use algorithms and data to recommend the most favorable aircraft for specific customers. User reviews, comments, and shared experience of aeronautical advice official information about user preferences on recommended systems. Due to the experience of computational models and small data, controlled decisions do not fall within a specific range. This proposal addresses data recommendation and parallel processing issues using supervised machine learning techniques. Large-scale decision-making techniques are used to find alternatives to implement different types of computing structures. It recommends operating systems such as variables or data reduction, data switch cleaning, and operation clustering.

Keywords Delay prediction · Aviation · Machine learning

1 Introduction

The airline trips are similar to store-sales consultants' forecast system in ARDPs, which ask about customer preferences and then show the aircraft. In e-commerce, the software does this automatically. It will start referring after checking the flight instructions. It is essential part of personalizing a Web site. Based on the algorithm and the data collected, this feature is called personal aviation advice ARDP, which

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The author(s), under exclusive license to Springer Nature Singapore Pte Ltd. 2021
© K. Singh et al. (eds.), *Proceedings of Integrated Intelligence Enable
Networks and Computing, Algorithms for Intelligent Systems*,
https://doi.org/10.1007/978-981-33-6307-6_25

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Structural Strength Monitoring System Practices Using Machine Learning



M. Vishnu Vardhana Rao and Aparna Chaparala

Abstract Structures are exceptionally helpless against impacts like natural effects, earthquakes, and typhoons. Along these lines, the organizer must know the damage and quality status of the structures in time so that essential maintenance is performed. More imaginative auxiliary damage identification systems connected to the current structures for Structural Strength Monitoring (SSM), particularly substantial scale structures, and many testing strategies are nondestructive. Considerations are attracted to how to utilize the present estimation information to create an outcome with less vulnerability, paying little intelligence to estimate clamors and natural assortments, such as evolving temperature, humidity, and load condition. This work presents two contributions. The role of sensors utilizes the Wireless Sensor Systems for diagnostic faults in the building. So Structural Strength Monitoring System (SSMS) utilizing Wireless Sensor Systems has considered as predominant research area because of its capacity to decrease the expenses related to the establishment and maintenance of SSMS frameworks and provides an extensive study of SSMS utilizing WSNs, drafting the calculations utilized in risk discovery and confinement, laying out system configuration difficulties. Another novel hybrid classification method which combines the features of Rough set (RS) with support vector machine (RS-SVM) and also with artificial neural network (RS-ANN). RS-SVM is used to classify the structures, and RS-ANN is used to predict the damage levels. The experiment results compared with the new SVM classifiers and identified that our approach got higher accuracy.

Keywords Rough set support vector machine (RS-SVM) · Rough set artificial neural network (RS-ANN) · Structural strength monitoring system (SSMS) · Wireless sensor systems (WSNs)

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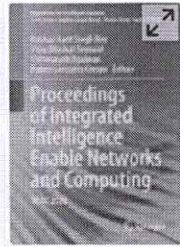
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Singh Mer et al. (eds.), *Proceedings of Integrated Intelligence Enable Networks and Computing, Algorithms for Intelligent Systems*
https://doi.org/10.1007/978-981-33-6307-6_26

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An Adaptive Deep Learning Model to Forecast Crimes

[C. Srinivasa Kumar](#) , [S. Ranga Swamy](#), [I. Navakanth](#) & [J. V. N. Raju](#)

Conference paper | [First Online: 24 April 2021](#)

613 Accesses

Part of the [Algorithms for Intelligent Systems](#) book series (AIS)

Abstract

Assessing crime is an important process as crime is on the rise these days. Assessing cybercrime can be a daunting task. It can be challenging to collect existing data and work on new techniques. In cybercrime, direct real-time assessment is obligatory. However, it is difficult to pinpoint when the



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